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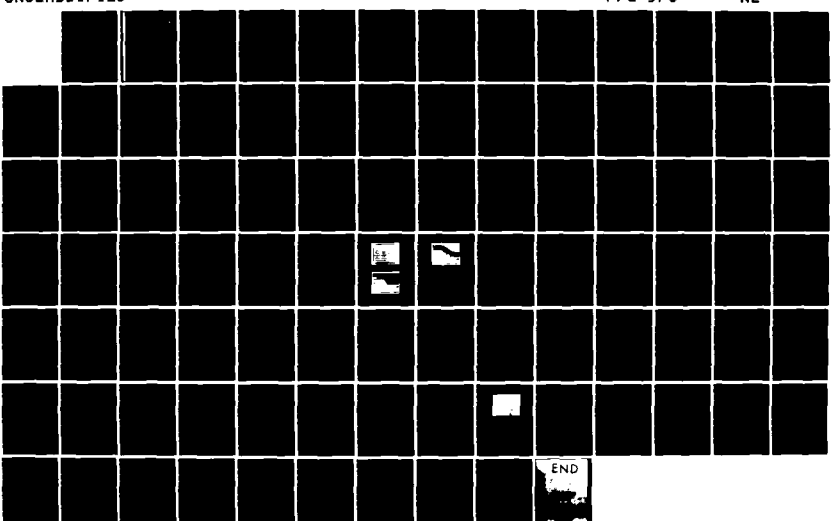

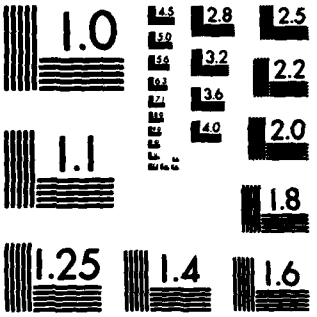

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STANFORD ELECTRONICS LABORATORIES

DEPARTMENT OF ELECTRICAL ENGINEERING
STANFORD UNIVERSITY · STANFORD, CA 94305

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This is the third annual report of the research under JSEP contract No. DAAG-81-K-0057.

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Table of Contents

List of Figures

List of Tables

INTRODUCTION

This report describes work performed under the Joint Services Electronics Program, sponsored by the Departments of the Air Force (Air Force Office of Scientific Research), Army (Army Research Office), and Navy (Office of Naval Research), under contract DAAG29-81-K-0057 at the Stanford Electronics Laboratories, Stanford University, Stanford, California.

The three most significant accomplishments, as determined by the Director, are summarized as:

1. *Real-Time Statistical Data Processing*

   The goals of this research program include focusing on methods for determining the number of sources when the signal is completely coherent with one or more interferences. A new approach to the problem of determining the number of sources for a passive array was developed [7]. The method is based on *information theoretic criteria* concepts for model selection. Rather than requiring the definition of thresholds (as needed in the conventional hypothesis testing approaches for determining the number of sources in the eigenstructure framework), the new approach does not require any *subjective* threshold settings. Simulation studies yield good results under varying situations including low signal to noise ratios, small number of data samples and closely spaced signals.

   The new approach is equally applicable in other areas where eigenstructure methods have been used. Some examples are determining the number sinusoids in time series data, the number of poles from the natural response of a linear system and the number of overlapped echoes in backscatter data typical in radar, etc.

2. *Physics and Technology of Submicron Devices*

   This research program was divided into a number of projects. Two of these projects have matured to the point that these seed projects have spawned new, larger projects which endeavor to carry these studies forward and to study the application of the capabilities shown to be possible with the work sponsored by this JSEP contract.

   One of the projects has been aimed at developing SIPOS (Semi-Insulating Poly Silicon) emitters for bipolar transistor applications [8, 6, 5]. Using heterojunction contacts to emitter regions as discussed in previous JSEP reports, the transistor current gain increased by an order of magnitude over that attainable with conventional diffused emittters and metal contacts. This makes substantial improvements in device performance and optimization of bipolar devices for VLSI applications possible. Follow-on work is expect to continue under a contract under negotiation with Sandia.

   In another of the projects, a mathematical analysis of the physics of trench-like isolation region structures resulted in new physical understanding of these structures and in an equation relating the leakage current to the radius of the interface [2, 1, 3]. The strong dependence of the corner effect on the radius was verified by the fabrication of several test transistors with different radii. Measurements of these transistors also demonstrated

the improved isolation properties with substrate bias and drain voltage. Burying the oxide and sharpening oxide corners means improved isolation and more compact VLSI layouts. This work is continuing under DARPA sponsorship on contracts MDA903-79-C-0257 and MDA903-84-K-0062.

3. *Signal Processing and Compression*

This research program was also divided into a number of projects. Of special interest is the work in vector quantization. The project has focused on three principal problems: The design of feedback vector quantizers for data compression, the design of adaptive vector quantizers for speech compression, and the extension of vector quantizer design algorithms to the design of combined quantization/classification distributed sensor networks. In the area of **Feedback Vector Quantizers**, a stochastic gradient algorithm for designing predictive vector quantizers (PVQ) was developed in order to get better codebooks and faster design speed. To further improve the performance, adaptive VQ's which combine the waveform coding techniques and linear predictive coding (LPC) techniques were studied.

Codebook and predictor design based on a stochastic gradient algorithm simultaneously improves the linear predictive coefficients and the vector quantizer in the feedback loop iteratively for a given training sequence. This provides better performance and faster convergence. Further details are reported in [4].

An NSF contract will be supporting the related theory of the finite state vector quantizers in the future. Related practical work is now being pursued at the University of California, Berkeley and at Bell Labs.

This report contains:

- Summaries of work for the JSEP-sponsored projects for the period April 1, 1983 through March 31, 1984.
- A List of JSEP Sponsored Publications through 31 March 1984 is included at the end of each summary.

References

1. S. H. Goodwin and J. D. Plummer Trench Isolation Technology and Device Physics. VLSI Symposium, IEEE, September, 1983.

2. S. Goodwin. Isolation Structures for VLSI -- Device Physics and Electrical Characteristics of Deep Groove Structures. Tech. Rept. TR # G725, Stanford Electronics Laboratories, January, 1984.

3. S. H. Goodwin and J. D. Plummer. "Electrical Performance and Physics of Isolation Region Structures for VLSI." *IEEE Trans. on Electron Devices ED-31* (July 1984).

4. Gray, R.M. "Vector Quantization." *IEEE ASSP Magazine* (April 1984).

5. Kwark,Y.H., and Swanson,R.M. Technology and Performance of SIPOS Heterojunction Emitters. Proc. 40th Annual Device Research Conference, IEEE, 1982. Conference Held at Ft. Collins, CO

6. Kwark,Y. and Swanson,R.M. "Optical Absorption of Thin SIPOS Films." *J. Electrochemical Soc.* 129, 1 (January 1982), 197-201.

7. Wax, M. and Kailath,T. Determining the Number of Signals by Akaike's Information Criterion. Proc. ICASSP, San Diego, CA, March, 1984, pp. 6.3.1-6.3.4.

8. Yablanovich, E., Swanson, R. M., and Kwark, Y. H. An n-SIPOS:p-SIPOS Homojunctionn and a SIPOS-Si-SIPOS double heterostructure. Proceedings 17th IEEE Photovoltaics Specialists Conference, 1984.

1. VERY LARGE SCALE INTEGRATION

1.1 Properties of Materials: Application of Channeling Radiation to a Study of the Properties of Materials

Principal Investigator: R. H. Pantell

1.1.1 Scientific Objectives

Our long term objective is to determine those crystal properties which can be studied by means of channeling radiation, and to relate these properties to experimental observations. We have successfully applied this technique to a variety of materials (Si, Ge, LiF, NaCl, W, and LiH), and in the future the emphasis will be on investigating defects and properties of electronic semiconductors, (Si, GaAs, and AlGaAs). These materials are important for their use respectively in VLSI, in high speed microwave and digital components, and in semiconductor lasers.

This approach, channeling radiation study of crystals, is nondestructive, and can be used to investigate electron distribution, crystal potentials, atomic vibrations, damage and defects, and anistropic properties. In comparison to the electron microscope (TEM, SEM or STEM), channeling radiation is applicable to much larger and thicker samples (up to 100 μm thick). Channeling radiation provides an alternative technique to x-ray diffraction for the determination of crystal parameters. Whereas x-ray measurements rely upon the accurate measurement of diffracted beam intensities, the channeling radiation technique involves a measurement of spectral peak positions, which can be determined more precisely.

During the next year we plan to perform the following:

- repeat the experiment with oxygen platelets in silicon and investigate the statistics of platelet structures and their properties. Oxygen in Si has been an important subject for many years because of enhanced gettering of metal ions in Si wafers with oxygen platelets.
- investigate clustering of dopants and defects in both AlGaAs and GaAs. This is an interesting subject because of the use of these materials in fast transistors utilized in advanced computers and in microwave structures.
- study the effects of damage induced in the above electronic semiconductors by both particle beams and electromagnetic radiation while the damage is occurring.
- investigate the above electronic semiconductor materials at low temperatures. By

reducing the crystal temperature, we can study the various characteristics of the materials as a function of temperature, such as thermal vibration amplitude, electron scattering, and electron distribution. These results may be of value in deciding whether low temperature operation of VLSI has sufficient advantages to justify the increased system complexity.

Channeling radiation provides a new tool for investigating the properties of crystals. We have begun to utilize this tool for both "perfect" crystals and crystals with defects, and we propose to extend our work to new materials and new types of defects.

1.1.2 Progress

During the past year we performed measurements of channeling radiation from 54 MeV electrons in Si with an oxygen platelet impurity; calculated potentials and eigenvalues for 17 MeV electrons in GaAs, AlGaAs, and AlAs; measured channeling radiation down to liquid nitrogen temperature; measured and compared electron channeling radiation form LiH and LiD; and measured 12.6 MeV electron channeling radiation from Si, diamond and LiF.

1.1.2.1 Channeling Radiation from Si with an Oxygen Platelet Impurity

Oxygen precipitation in silicon has been the subject of many studies utilizing different techniques. [1, 10] Oxygen is the main impurity present in Czochralski (CZ) grown silicon and its presence may directly or indirectly affect the electronic properties of the device.

We have measured 54 MeV electron channeling radiation from a 130 μm thick Si crystal with oxygen platelets. The wafer was subjected to a 750°C anneal under dry O_2 for 100 hours, and the oxygen concentration in this crystal was measured at 26 ppm. This crystal shows the following defects from high resolution TEM pictures.

1. Thin (10-30 angstroms) platelets of $\simeq$ 200-1500 angstroms diameter parallel to (100) Si planes.

2. Small stacking faults lying in (111) planes in the vicinity of the (100) planar silica defect. A TEM photograph of a lattice with a (100) platelet after a 750°C anneal is shown in Fig. 1-1

The 54 MeV electron channeling radiation spectra from the Si + 0 crystal are shown in Fig. 1-2, and compared to those from a 40 μm thick Si crystal without the oxygen platelets. Figs. 1-2(a)-(c) are the spectra from (100), (110), and (111) planes, respectively. Heavy dots are the data from the Si + 0 crystal, and light dots are from Si. The (100) and (111) spectra from the two crystals are not very different, however, the (110) plane spectrum from the Si + 0 crystal shows large linewidth broadening

compared with that from Si. Also, there are peak energy down-shifts in 1→0 and 2→1 transitions (Table 1-1). The transition energy changes in (110) planes are probably not due to the thickness differences between the two crystals, because this effect was not observable in (100) and (111) planes.

We previously reported the downshift of radiation energies from the (100) plane in diamond with a nitrogen defect [8]. This is a reasonable result considering the distortion in the (100) plane resulting from the platelet. It is not clear why we observed the downshift in the (110) plane in the Si + 0 crystal rather than from the (100) plane. This experiment will be repeated with a thinner Si + 0 (30 micron) crystal and will be studied further.

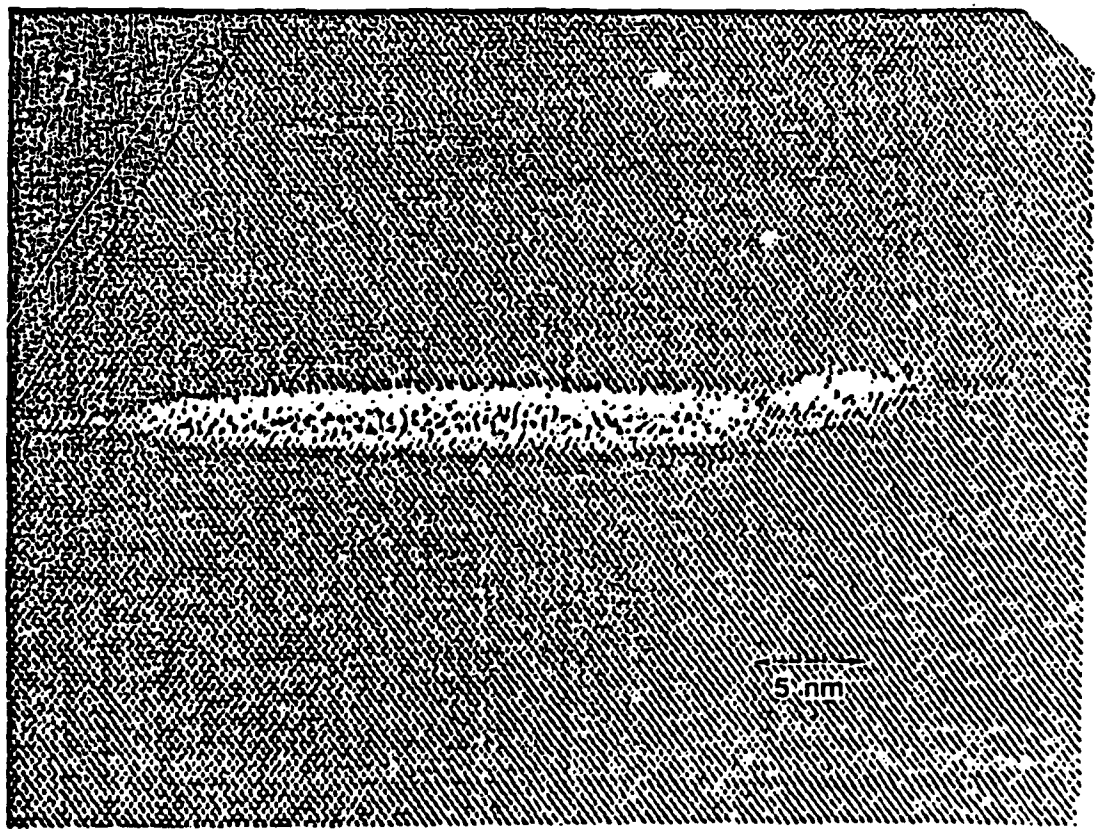


Figure 1-1: *High resolution TEM images of thermally induced microdefects in Si*

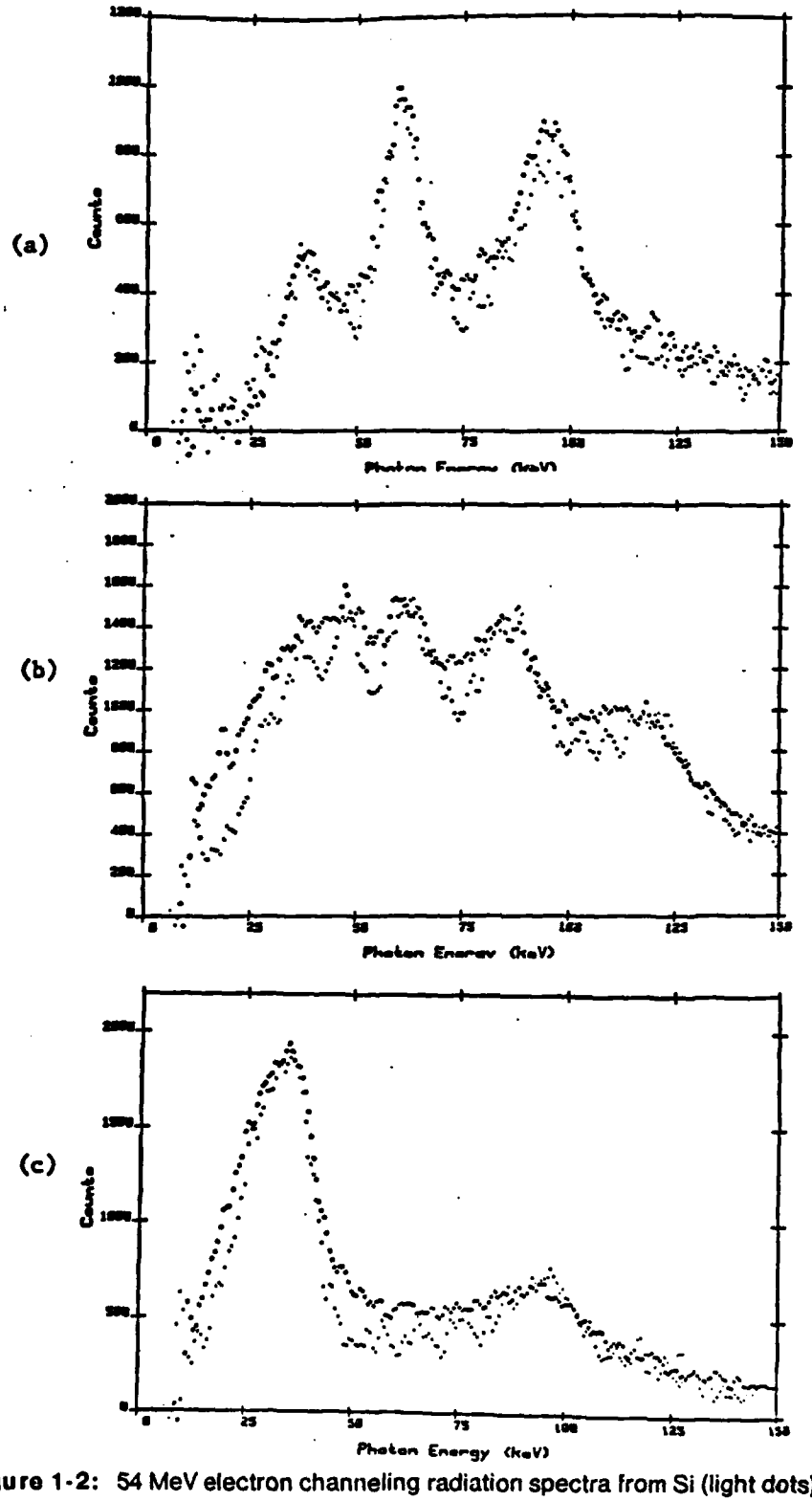


Figure 1-2: 54 MeV electron channeling radiation spectra from Si (light dots) and Si + O (heavy dots)

Table 1-1: Comparison of Peak Energy and Linewidth from Si with and without Platelets

Plane	Transition	Si (40μm)		Si+O(130μm)	
		Peak Energy (keV)	Linewidth (keV)	Peak Energy (keV)	Linewidth (keV)
	1→0	95.8±1.2	17.4±0.6	94.8±1.2	14.5±0.4
(100)	2→1	60.8±0.8	10.3±0.4	60.5±0.8	10.6±0.5
	3→2	37.7±1.2	11.0±0.8	37.6±1.0	10.3±0.8
(110)	1→0	121.7±1.6	18.1±0.6	116.1±2.0	21.3±1.0
	2→1	87.1±1.2	11.9±0.4	86.4±1.2	14.8±0.8
	3→2	62.6±1.0	10.3±0.4	62.1±1.2	9.0±0.6
	4→3	48.0±0.8	7.7±0.4	48.8±1.0	8.4±0.6
	5→4	37.1±0.8	7.1±0.4	37.7±0.8	9.0±0.8
	6→5	28.5±0.8	4.6±0.6	28.8±0.8	5.8±0.8
(111)	Small Peak	95.0±1.0	18.8±0.6	93.6±1.0	21.6±0.6
	Large Peak	36.0±0.6	25.5±0.3	35.0±0.4	29.0±0.3

1.1.2.2 Calculated Potentials and Eigenvalues in GaAs, AlGaAs, and AlAs

GaAs-AlGaAs is an important material because of its use in the superfast computers [6] and in diode lasers [7] for fiber communication. There have been some interesting studies about clustering of Al [4, 5] and strain [2] in these materials. These phenomena should be easily observable by both positron and electron channeling radiation.

Figure 1-3 shows the calculated planar potentials and eigenvalues for 17 MeV electrons channeled by (100) planes in GaAs, $Al_{0.3}$ $Ga_{0.7}$ As, and AlAs. Fig. 1-4 shows the calculated spectra, assuming 20 micron of crystal thickness. In $Al_{0.3}$ $Ga_{0.7}$ As, if the Al is not uniformly distributed or is clustered, one will not observe a spectral peak and perhaps there will be no channeling radiation at all.

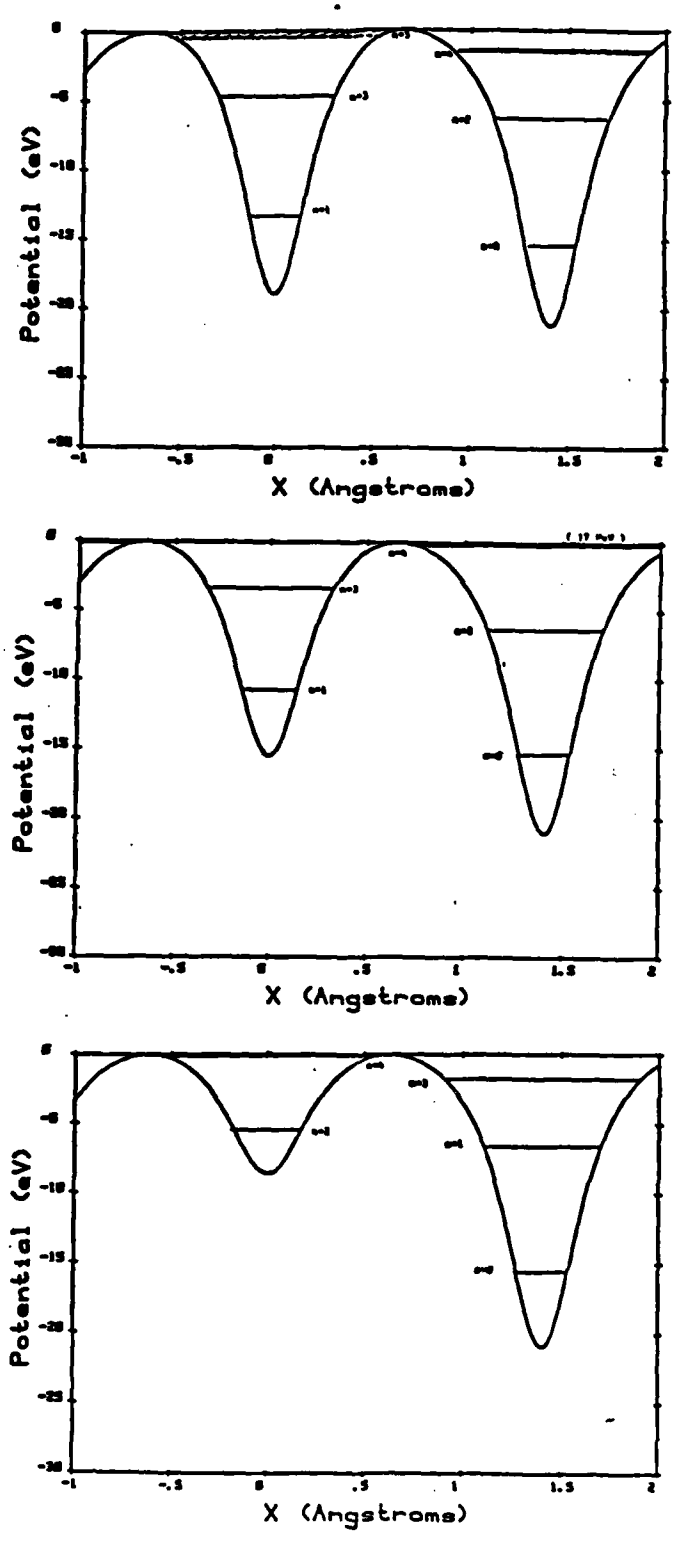
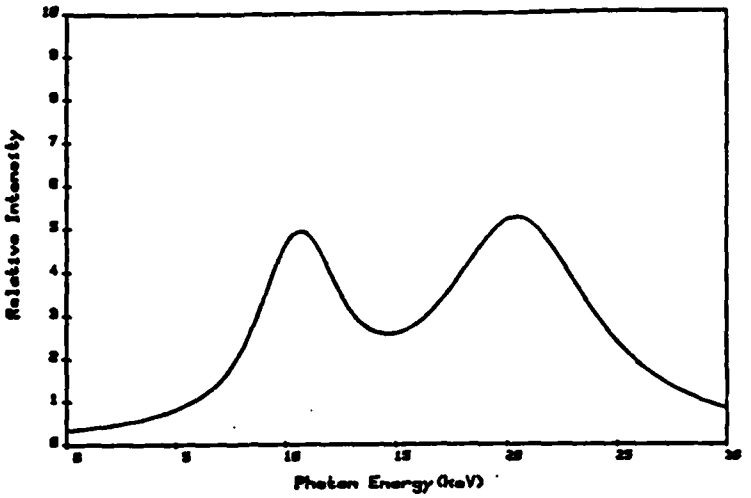
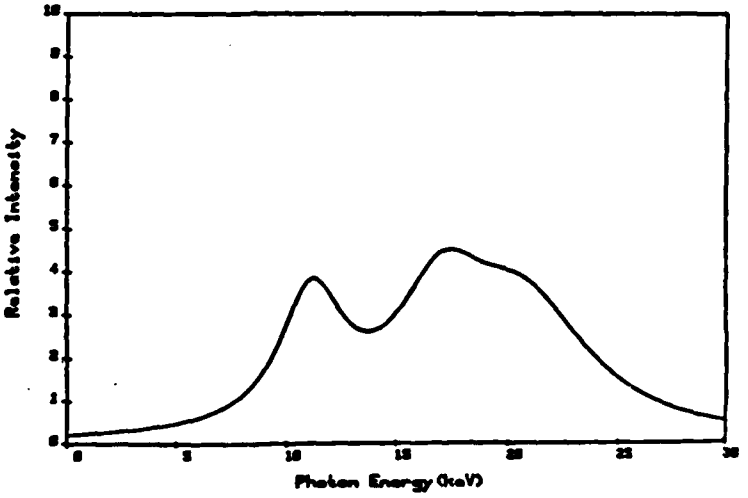


Figure 1-3: (100) potentials and eigen values for 17 MeV electrons in a) GaAs, b)$Al_{0.3}$ $Ga_{0.7}$ As and c) AlAs.

(a)



(b)



(c)

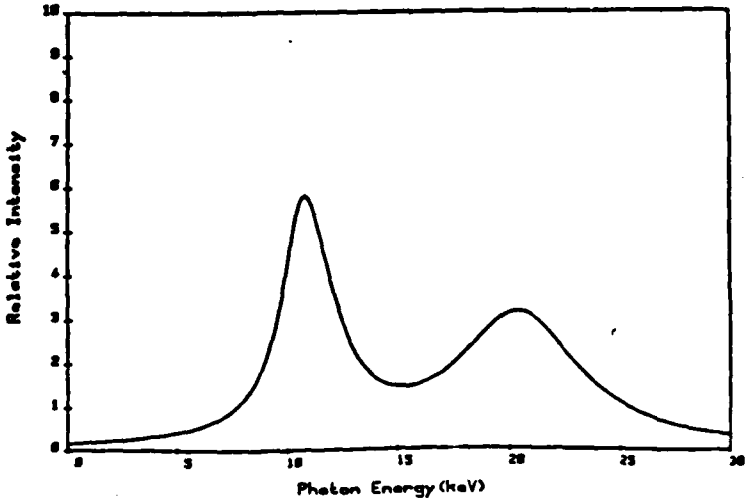


Figure 1-4: Calculated spectra for 17 MeV electrons in a) GaAs, b) $Al_{0.3}Ga_{0.7}As$ and c) AlAs.

1.1.2.3 Low Temperature Channeling Radiation

We measured 54 MeV electron channeling radiation from a Si crystal as a function of temperature. For electron channeling, the thermal vibration of the atoms, which causes transitions between eigen states as well as dechanneling, is the primary contribution to linewidth. At lower temperature the linewidth is reduced, since the thermal vibration of atoms decreases with temperature. Another effect of cooling is to shift the spectral lines to higher frequencies. The potential well for a fixed atom is deeper than the well for a vibrating atom, and in ther former case there is greater separation between energy eigen values.

Figures 1-5(a) and (b) show the 54 MeV electron channeling radiation spectra from (100) and (110) planes in a Si crystal at room temperature and at a low temperature. Heavy dots are low temperature data (-190°C for (100) plane and -180°C for (110)), and room temperature data are light dots. We can observe the 1→0 transition energy shift very clearly. Also, some line narrowing can be noticed. Figures 1-6(a) and (b) show the measured and calculated channeling radiation peak energy as a function of temperature, using the Debye approximation [3] to estimate the thermal vibration amplitude.

For both the (100) and (110) planes, the 1→0 transition shows the greatest discrepancy between the theoretical calculation and the experimental result. However, the higher n-values the agreement is better. From our experimental results, we can deduce a Debye temperature of 475°K, which is somewhat lower than the value given in the literature [543°K] [3]. In other words, our experiment shows larger atomic vibration amplitudes than the published values (0.085 angstroms vs 0.075 angstroms at room temperature).

Figures 1-7(a) and (b) show the measured linewidths for transitions in (100) and (110) planes as a function of temperature. The dotted lines are the best fit curves. As we expected, the linewidth decreases as the crystal temperature deceases. The effect is strongest for 1→0 transitions, since these states lie deepest in the potential well and have the most overlap with the vibrating atoms.

1.1.2.4 Electron Channeling Radiation from LiH and LiD

We measured 54 MeV electron channeling radiation from LiH and LiD crystals. This is the first time that channeling radiation has been used to identify isotopes in crystals. Figure 1-8 shows the measured spectra from (100) planes in LiH and LiD crystals. The spectrum from LiH is in light dots and heavy dots are for LiD. The thicknesses of the crystals are 190 microns and 350 microns for LiH and LiD, respectively. From the experimental results, the radiation peak energies from LiD are higher

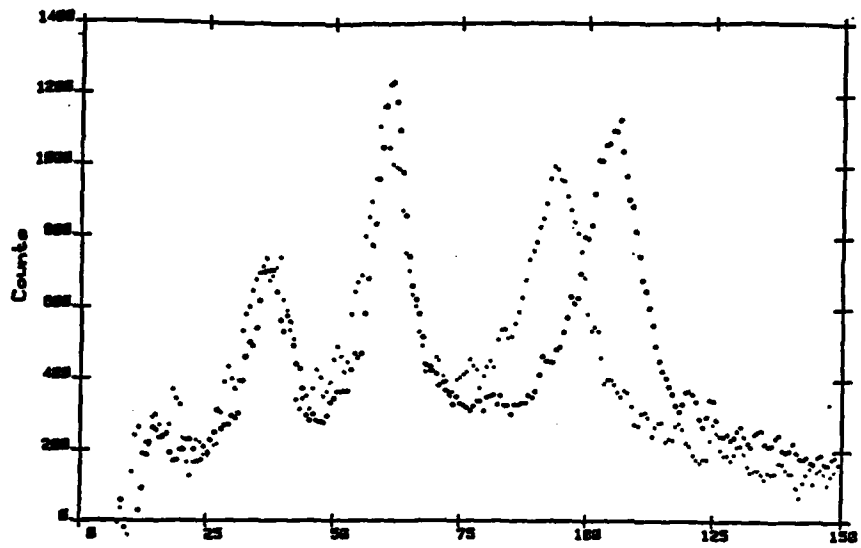


Figure 5. (a)

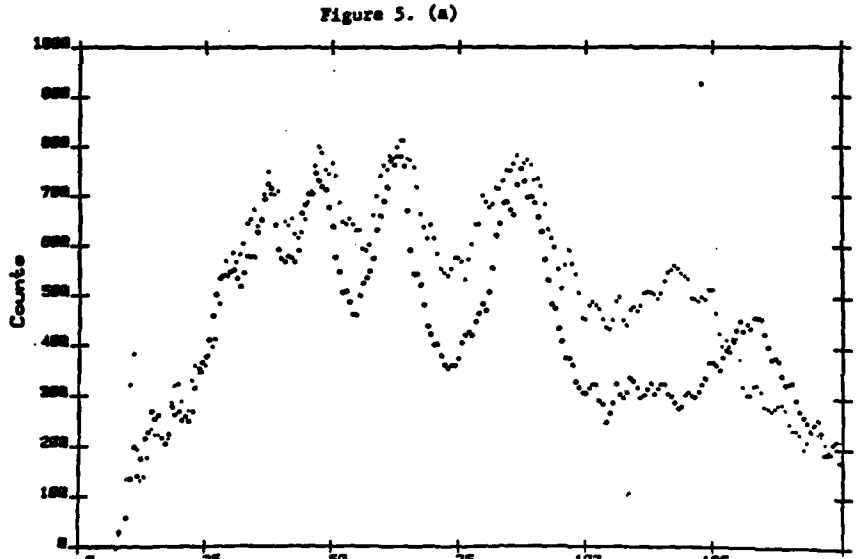


Figure 5. (b)

Figure 1-5: 54 MeV electron channeling radiation spectra from Si,
a) (100) plane at -190°C (heavy dots) and 5°C (light dots).
b) (110) plane at -180°C (heavy dots) and 7°C (light dots).

than LiH, which is contrary to what we calculated. Table 1-2 shows the calculated and measured

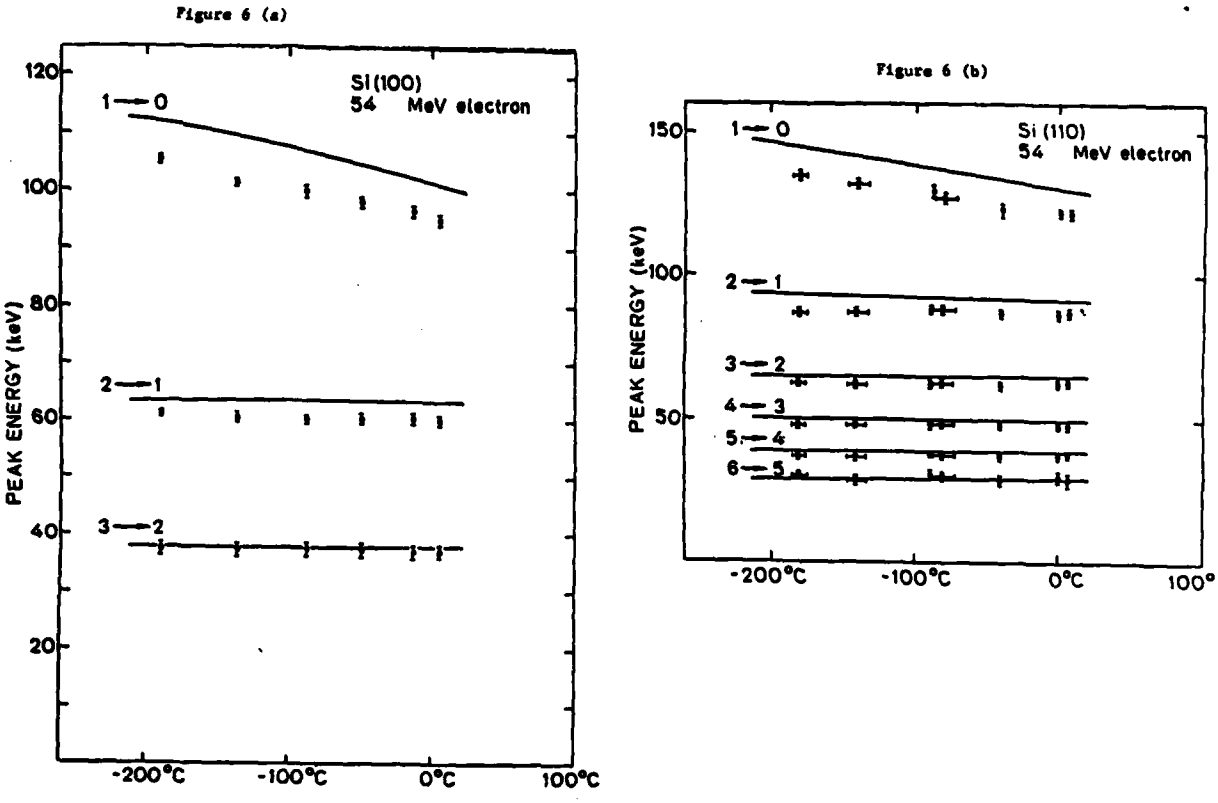


Figure 1-6: 54 MeV electron channeling radiation peak energy vs. temperature in Si. a) (100) and b) (110) plane. Solid curves show theoretical values.

channeling radiation energies from LiH and LiD. In this calculation, the published thermal vibration amplitudes [9] were used.

For both LiH and LiD, the calculations do not fit very well; the calculated values are too high for LiH and are low for LiD. The most significant difference is that, based upon theoretical calculations, the radiated peak energies from LiH are higher than those from LiD, whereas the experimental results show the opposite trend.

From these experimental results, we can conclude that the atomic thermal vibrations for LiD are smaller than those for LiH. We improved the fit to our data by changing the thermal vibration amplitudes based upon minimizing the mean square error between theory and experiment. Table 1-3 gives the calculated values for the modified thermal amplitudes along with the measured values. The agreement is much better than that which can be obtained using the published values for vibrational amplitudes.

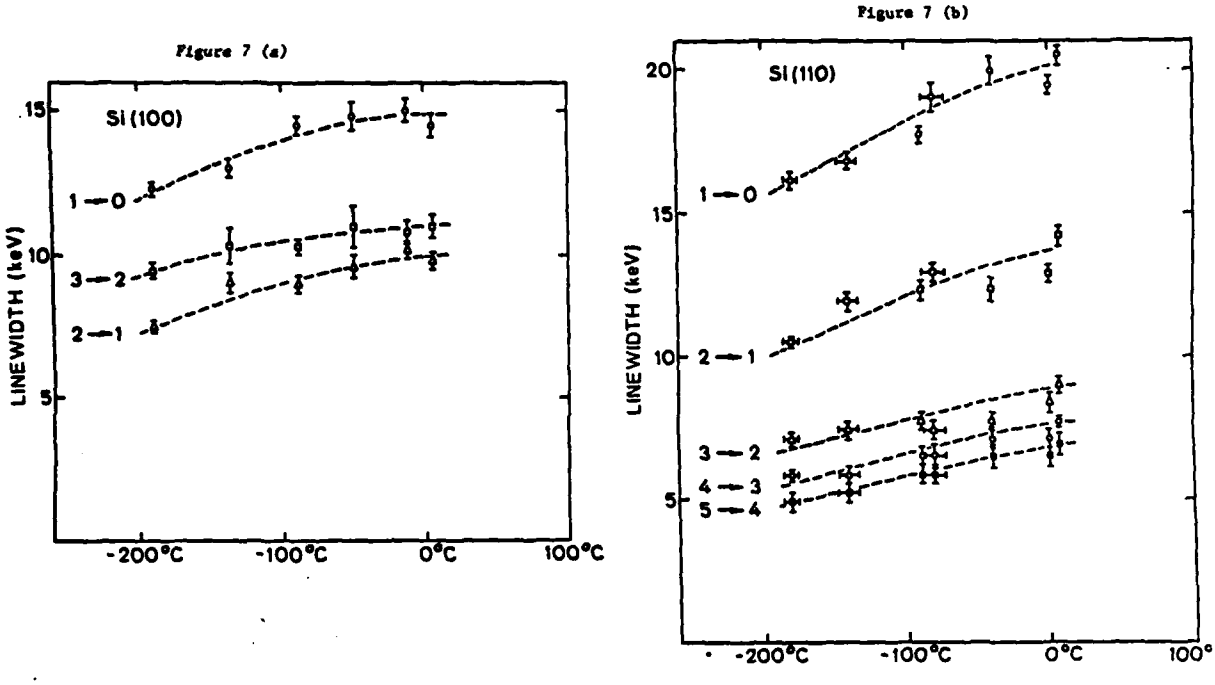


Figure 1-7: 54 MeV electron channeling radiation linewidth vs. temperature in Si a) (100) and b) (110) planes. Dotted lines are the best fit curves.

1.1.2.5 12.6 MeV Electron Channeling Radiation from Diamond, Si and LiF

This experiment was done to test whether we can obtain good results for lower energy electrons from the accelerator at LLNL, since we need lower beam energies to analyze high Z semiconductor materials (e.g. GaAs) studies. Figure 1-9 illustrates the axial channeling spectra from <100>, <110> and <111> axes in diamond. These results indicate excellent channeling radiation spectra, and prove that the beam quality is comparable or better than that for the 30-60 MeV electrons we have used previously.

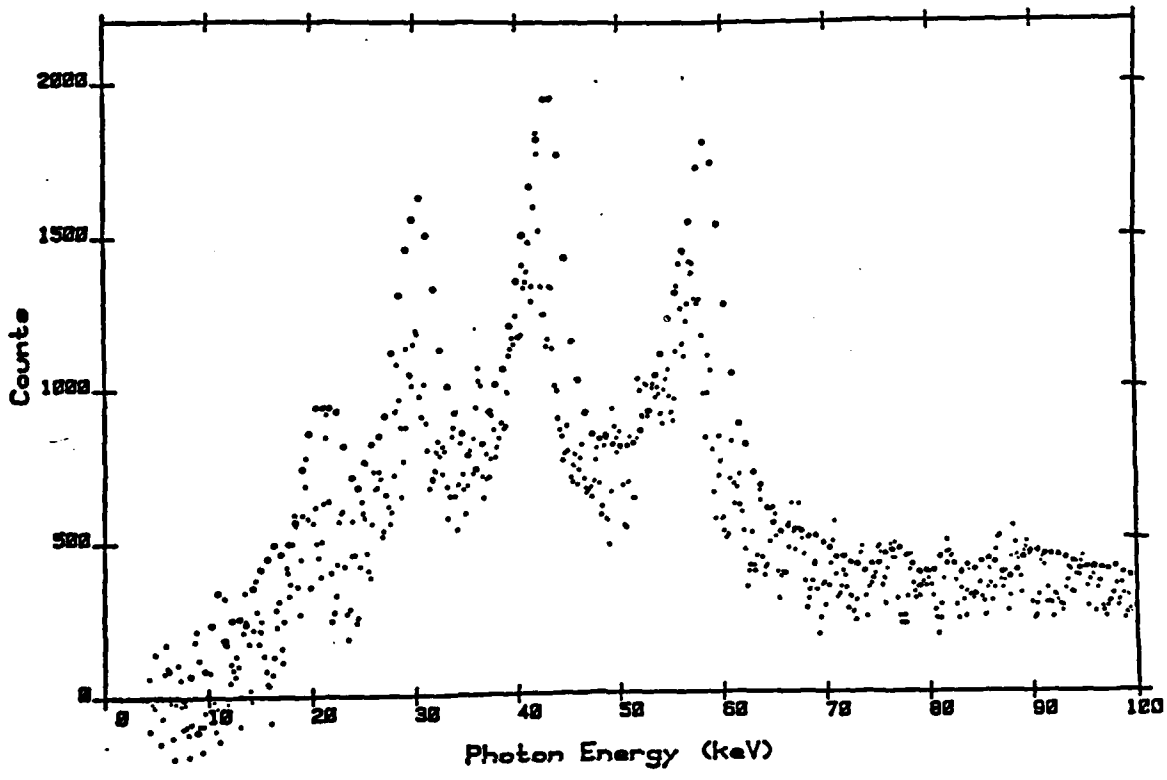


Figure 1-8: 54 MeV electron channeling radiation spectra from (100) planes in LiH (light dots) and LiD (heavy dots)

Table 1-2: Comparison of the Calculated and Measured Energies for LiH and LiD

		Calculated*(KeV)		Measured (KeV)	
Plane	Transition	LiH	LiD	LiH	LiD
(100)	1→0	62.4	55.8	57.0∓0.6	58.3∓0.4
	2→1	45.6	43.6	41.8∓0.4	43.6∓0.3
	3→2	33.1	32.9	29.6∓0.4	30.3∓0.3
	4→3	23.6	23.7	21.1∓0.5	21.2∓0.4
(110)	1→0	47.7	42.7	41.3∓0.5	45.3∓0.4
	2→1	29.4	28.3	26.3∓0.5	28.1∓0.3
(111)	1→0	53.6	47.0	52.0∓0.4	52.8∓0.4
	3→1	32.6	31.5	36.5∓0.4	37.4∓0.3
	2→1	24.3	25.5	26.0∓0.4	25.1∓0.3

*Thermal vibration amplitudes [9]

LiH Li: 0.113 angstroms LiD Li: 0.147 angstroms

H: 0.153 angstroms D: 0.178 angstroms

Table 1-3: Comparison of Calculated Energies Using Modified Thermal Amplitude and Measured Energies

		Calculated* (Modified)		Measured	
Plane	Transition	LiH	LiD	LiH	LiD
(100)	1→0	56.8	59.1	57.0∓0.6	58.3∓0.4
	2→1	42.3	44.2	41.8∓0.4	43.6∓0.3
	3→2	31.5	32.8	29.6∓0.4	30.3∓0.3
	4→3	23.0	23.7	21.1∓0.5	21.2∓0.4
(110)	1→0	43.1	45.1	41.3∓0.5	45.3∓0.4
	2→1	26.7	28.3	26.3∓0.5	28.1∓0.3
(111)	1→0	51.6	52.4	52.0∓0.4	52.8∓0.4
	3→1	33.9	33.1	36.5∓0.4	37.4∓0.3
	2→1	30.0	28.5	26.0∓0.4	25.1∓0.3

*Thermal vibration amplitudes used:

LiH Li: 0.12 angstroms LiD Li: 0.12 angstroms

H: 0.24 angstroms D: 0.20 angstroms

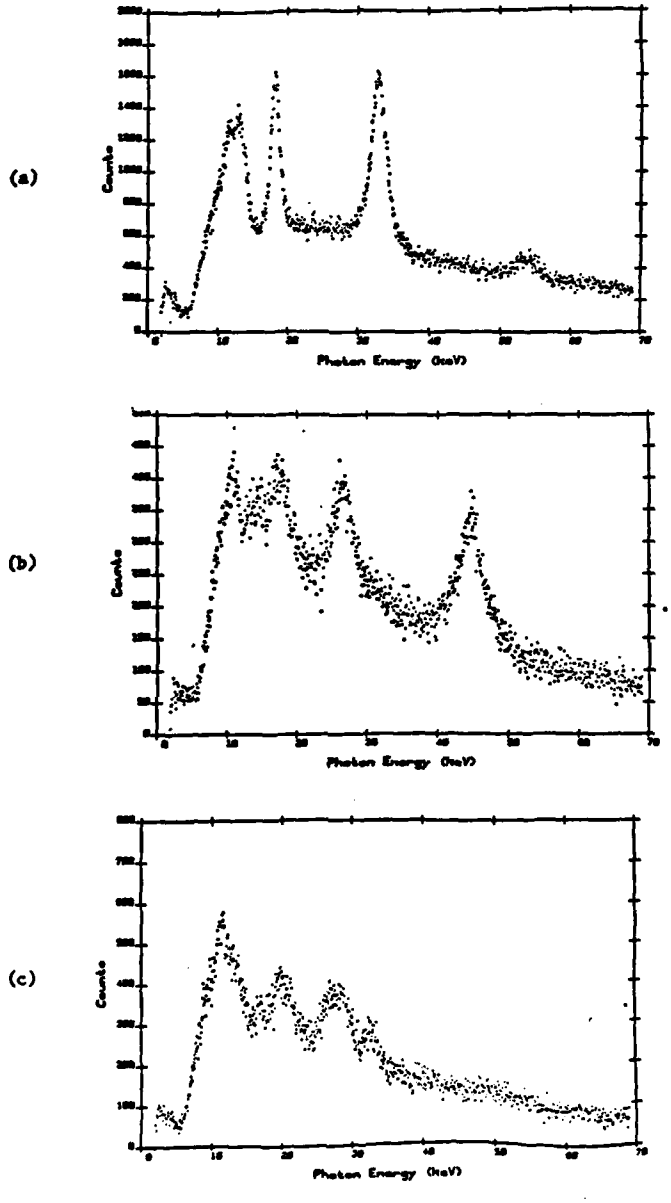


Figure 1-9: 12.6 MeV electron channeling radiation spectra from Diamond a) <100>, b) <110>, and c) <111> axis.

1.1.3 References

1. Bourret,A, Thibault-Desseaux,J. and Seidman,D. N. "Early Stages of Oxygen Segregation and Precipitation in Silicon." *J. Appl. Phys. 55* (1984), 825.

2. Chu,W. K., Ellison,J. A., Picraux,S. T., Biefeld,R. M. and Osbourn,G. C. "Resonance between the wavelength of planar-channeled particles and the period of strained-layer superlattices." *Phys. Rev. Lett. 52* (1984), 125.

3. Gemmell.D. S. "Channeling and related effects in the motion of charges particles through crystals." *Rev. Mod. Phys. 46* (1974), 129.

4. Holonyak, Jr.,N., Laidig,W. D., Vojak,B. A., Hess,K., Coleman,J. J., Dapkus,P. D. and Bardeen,J. "Alloy clustering in $Al_xGa_{1-x}As$ - GaAs quantum-well hetrostructures." *Phys. Rev. Lett. 45* (1980), 1703.

5. Miller,R. C., Weisbuch,C., Gossard,A. C. "Alloy clustering in $Al_xGa_{1-x}As$." *Phys. Rev. Lett. 46* (1981), 1042.

6. Morkoc,H. and Solomon,P. M. "The HEMT: a superfast transistor." *IEEE Spectrum* (February 1984), 28.

7. Olsson,N. A. and Tsang,W. T. "Transient effects in external cavity semiconductor lasers." *IEEE J. Quant. Elect. QE-19* (1983), 1479.

8. Park,H., Pantell,R.H., Swent,R.L., Kephart,J.O., Berman,B.L., Datz,S., and Fearick,R.W. "Comparison of Channeling Radiation from Diamonds with and without Platelets." *J. Appl. Phys. 55* (1984), 358-364. Sponsored by JSEP

9. *International Tables for X-Ray Crystallography.* 1959.

10. Yamatomo,N., Petroff,P. M. and Patel,J. R. "Rod-like defects in oxygen-rich Czochralski grown silicon." *J. Appl. Phys 54* (1983), 3475.

1.1.4 Recent JSEP Publications

1. Andersen,J.U., Bonderup,E., and Pantell,R.H. "Channeling Radiation." *Annual Rev. of Nuc. and Part. Sci. 33* (1983), 453-504. Sponsored by JSEP

2. Berman,B.L., Datz,S., Fearick,R.W., Swent,R.L., Pantell,R.H., Park,H., Kephart,J.O., and Klein,R.K. "Planar Channeling Radiation from Relativistic Positrons and Electrons in LiF." *Nucl. Instrum. Meth. B2* (1984), 90-94. Sponsored by JSEP

3. Datz,S., Fearick,R.W., Park,H., Pantell,R.H., Swent,R.L., Kephart,J.O., and Berman,B.L. "Electron and Positron Channeling Radiation from Type-Ia and Type-IIa Diamonds." *Nucl. Instrum. Meth. B2* (1984), 74-79. Sponsored by JSEP

4. Klein,R.K., Swent,R.L., Pantell,R.H., Park,H., Kephart,J.O., Berman,B.L., Datz,S., and Fearick,R.W. Electron Channeling Radiation in Diamond. Submitted to Phys. Rev. B, 1984 -- Sponsored by JSEP

5. Park,H., Kephart,J.O., Klein,R.K., Pantell,R.H., Berman,B.L., Datz,S., and Swent,R.L. Electron Channeling Radiation from Diamond with and without Platelets. Submitted to J. Appl. Phys., 1984, sponsored by JSEP

1.2 PHYSICS AND TECHNOLOGY OF SUBMICRON DEVICES

Principal Investigators: C.R. Helms, R.F.W. Pease, J.D. Plummer, W.E. Spicer, R.M. Swanson, J.S. Harris

Introduction

This research program is divided into a number of projects which are described separately below, including progress in each area during the past year and an outline of future plans. The first three, which report research under the direction of J.D. Plummer, are closely connected in that they are aimed at submicron VLSI devices.

In any MOS or bipolar integrated circuit, there are three generic types of structures. The first is the active switching/amplifying device. We are investigating the characteristics of alternative gate dielectrics for submicron NMOS and CMOS circuits. Thermally grown Si_3N_4 and SiO_2/Si_3N_4 composites appear to have significant advantages over SiO_2. This first project is aimed at evaluating material properties and corresponding device characteristics associated with this alternative dielectric.

The second generic type is a parasitic device and is the result of the local-oxidation techniques commonly used for device-to-device isolation. Such isolation is generally achieved in both bipolar and MOS integrated circuits through selective field oxidation coupled with self-aligned ion-implanted channel stops. Despite its current technological dominance, this isolation technique will be inadequate as device geometries approach 1 μm and, ultimately, submicron sizes. As a result, the scientific objectives of this second project are to:

1. use two-dimensional numerical simulation to determine and better understand the limits of local-oxidation device-isolation schemes and

2. investigate, both theoretically and experimentally, isolation techniques that may improve the isolation characteristics at feature sizes of ≤ 1 μm.

The third generic type is generally a passive load element which, in bipolar circuits, often takes the form of diffused or ion-implanted resistors. In NMOS circuits, the most common device is a polysilicon resistor. Polysilicon layers are also widely used as gate electrodes and for interconnections in MOS circuits. In this third project, we are investigating the limiting behavior of polycrystalline-silicon layers when they are defined with lateral and vertical dimensions comparable to the grain sizes in the material. The specific project under investigation is the sensitivity of Si/SiO_2 interface properties to ambient conditions when the interface is located under a polysilicon electrode.

We are attempting to determine the extent to which such interfaces are sensitive to surrounding ambients and in particular have looked at the properties of interface charges in small 2D structures.

In summary, we are engaged in a coherent investigation of the problems of submicron silicon integrated circuits, and the three projects are aimed at the three key components of any modern silicon circuit. Our intent is to establish a scientific basis for understanding and circumventing problems that may occur in scaling the three generic structures to submicron dimensions.

1.2.1 Electrical Performance and Physics of Isolation Region Structures for VLSI

Investigators: S. Goodwin, J. Plummer

1.2.1.1 Scientific Objectives

Virtually all modern MOS and bipolar integrated circuits use the local oxidation of silicon to isolate laterally between devices [1]. This isolation structure is typically formed by doping the field region using ion implantation followed by the growth of a thick oxide in the field region. The active device regions are protected from these steps by a masking layer of silicon nitride which is subsequently removed. The parasitic device that is formed comprises a source and drain from the source/drains of two adjacent active transistors and a gate made of an interconnection wire of polysilicon or metal. Good isolation entails that the parasitic device be turned off and conduct a minimum of current, which the increased doping and thicker oxide provide. With the parasitic transistor conducting a minimum of current, there is less crosstalk, less leakage from storage nodes, and less unwanted interaction between the active transistors. This technique of LOCOS isolation has certain advantages such as: the self-alignment of the field oxide to the more heavily doped channel stop, ion implantation of the channel stop to allow an optimum choice of substrate doping for the active devices, and the reduction of step height between the field and active device regions.

The LOCOS process has the undesirable by-product of a "bird's beak" due to lateral oxidation, which consumes chip area and therefore reduces device packing density. Another drawback is the lateral diffusion of the channel stop implant during the field oxidation which can also reduce the packing density by encroaching on active device channel regions and thereby requiring larger drawn device dimensions. Lateral channel stop diffusion also degrades the source/drain to substrate capacitance. Several recent papers have addressed technological alternatives to the LOCOS process, to circumvent these problems. The proposed alternative technologies can be divided roughly into two groups. One group is a return to the previous technique of a planar oxide/semiconductor interface with different oxide thicknesses above the interface. This can be

accomplished by growing a thick field oxide everywhere and then removing the oxide in the active device regions [14], or by depositing polysilicon and selectively oxidizing it into the field oxide [10]. Strict attention must be paid to controlling the step up to the field regions and doping of the field regions. The other group controls the lateral growth of the oxide during LOCOS with different processing [4, 8, 9, 2, 13]. These processing variations utilize different configurations of silicon nitride, or deposited oxides. We have investigated in this work some of the implications for electrical performance that these new isolation structures imply. By analyzing their physics of operation, the electrical characteristics can be predicted for new generations of devices. These predictions are experimentally verified through the fabrication of several "trench-like" structures. Both new technology and a better understanding of isolation region physics will be necessary to solve the isolation problems in submicron structures.

1.2.1.2 Progress

Computer Simulations

To obtain a preliminary understanding of the device physics, we chose to use computer simulations for flexibility and speed. Recognizing the inherent two-dimensional nature, the abundance of non-planar surfaces, and the normal operation of isolation devices in the subthreshold regime, we used GEMINI, a program that solves Poisson's equation in two dimensions [7]. GEMINI can be used to generate plots of the potential in the semiconductor along the current path. This aids in the understanding of the device operation since in the subthreshold regime, the drain current is controlled by the injection of carriers over a potential barrier and is related exponentially to the height of the barrier.

The first series of simulations compared two variations of the local oxidation technique, a semi-recessed and a fully-recessed structure as shown in Figure 1-10. The two devices were identical, except in the fully-recessed structure the silicon had been etched in the field regions prior to the field oxidation. These structures are somewhat ideal representations of actual isolation region structures, and were chosen to simplify the initial analysis. More realistic structures will be considered later in the experimental results section of this report. The two structures in the figure have the same oxide thickness, the same doping concentration, and the same junction depths; so we were surprised to find distinctly different electrical characteristics. Comparing their calculated $\log(I_D)$ vs. V_{GS} curves, the fully-recessed device conducted less current because of a flatter subthreshold slope, and hence had better isolation properties.

Examining the possible causes for this difference, we focussed on the corner of the field oxide and

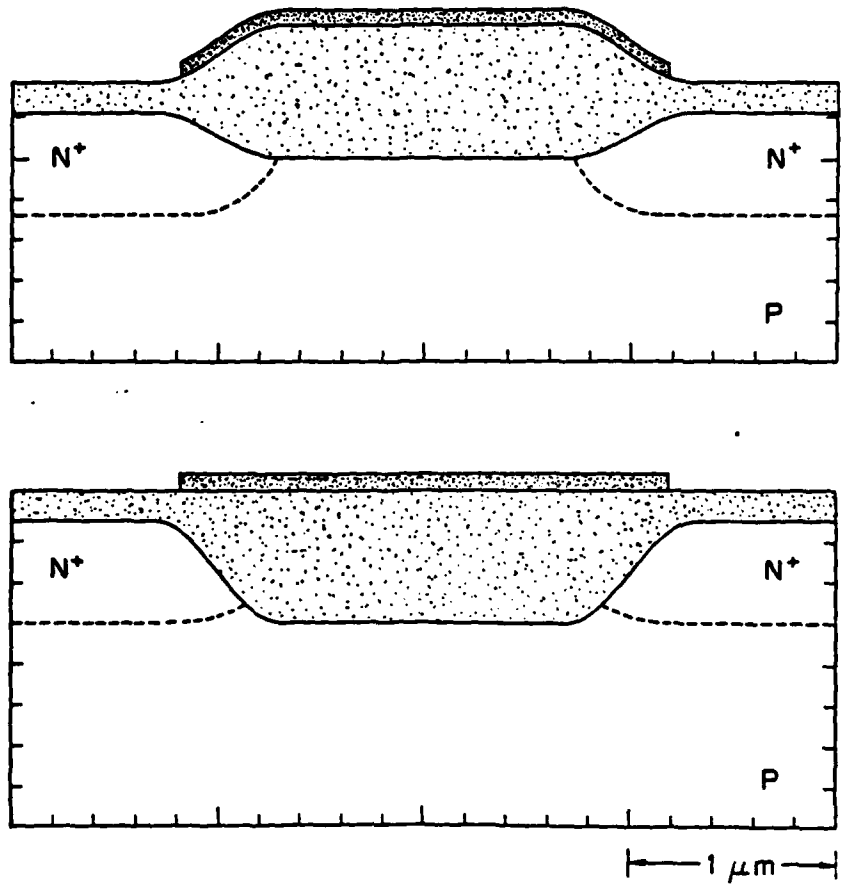
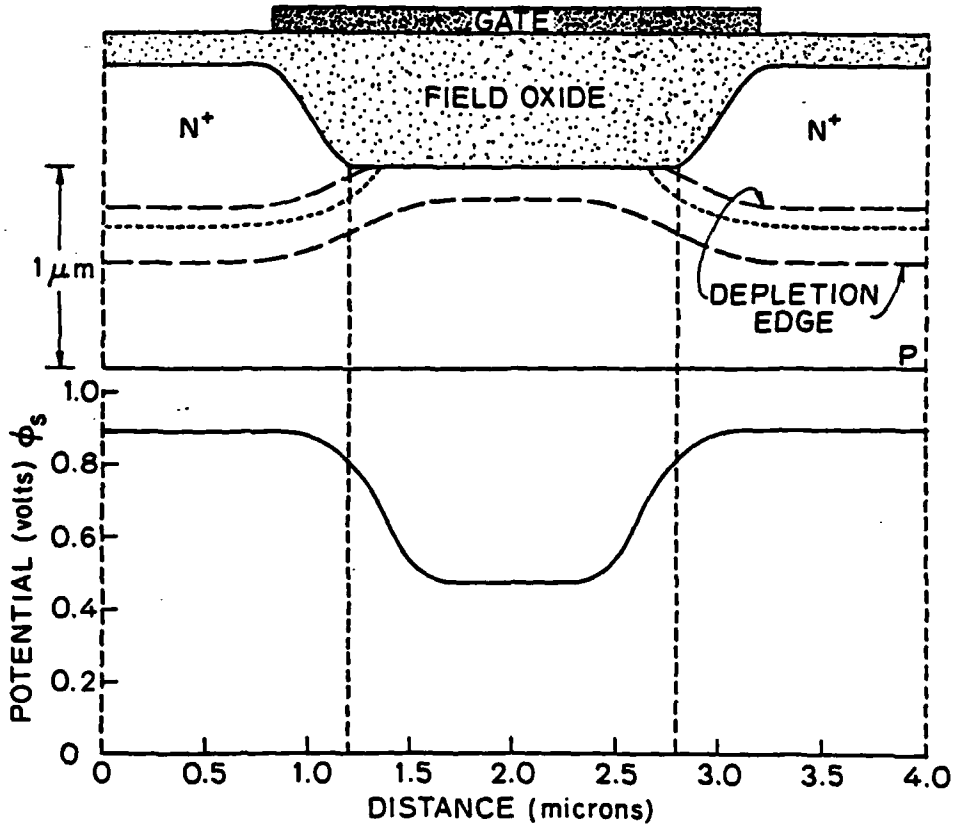


Figure 1-10: Initially simulated isolation devices with different I--V characteristics; semi-recessed, top, and fully-recessed, bottom. T_{ox} = 6500 Angstroms, x_j = 0.5 μm.

the different configurations of the nearby source and drain. Extending the channel of an isolation device around the oxide corner provides significant improvement in isolation due to geometrical reasons. To understand this, examine a normal device whose source and drain junctions extend below the oxide/semiconductor interface, as shown in Figure 1-11. Here the channel does not include the corners and standard one-dimensional theory applies. As the calculated plot of surface potential along the Si/SiO_2 interface shows, there is a potential barrier centered under the gate. As the gate voltage is increased, the height of the barrier decreases, and more current is able to surmount the barrier and reach the drain.

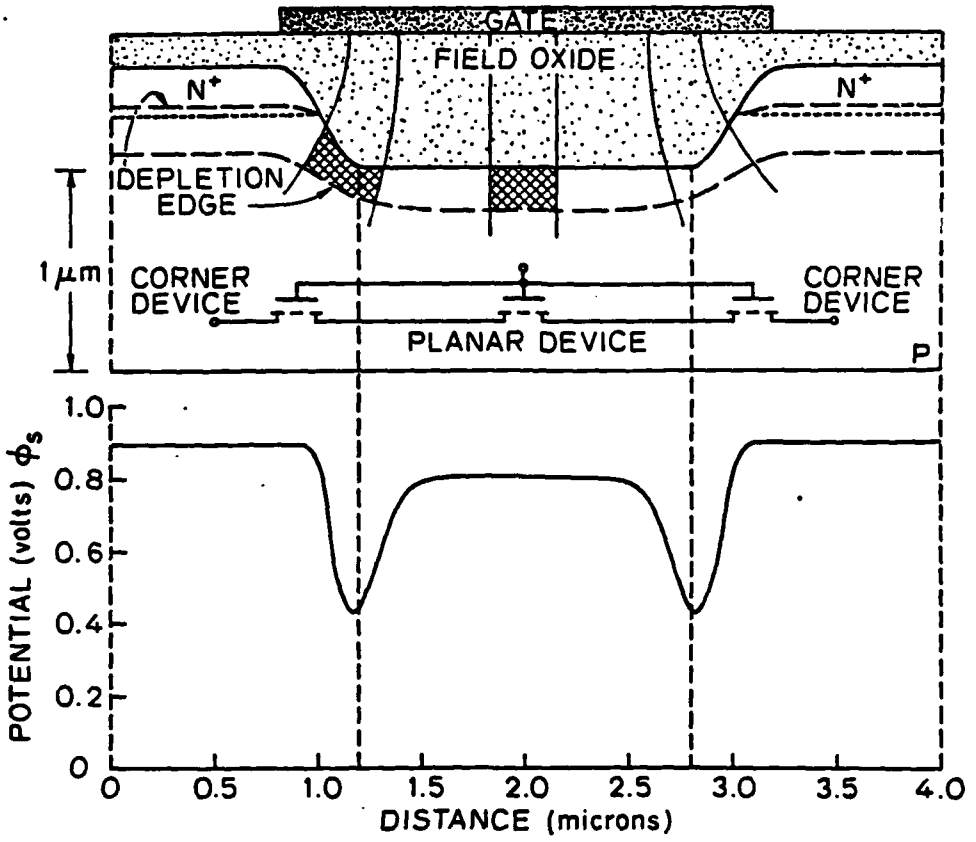
Figure 1-12 shows the identical device except the source and drain junctions are now much shallower, lying above the oxide/semiconductor interface. By pulling these junctions up, the oxide corners have been "exposed" and incorporated into the channel. Now the current flow and device physics become very two-dimensional in nature. One-dimensional theory fails to hold, as seen by the



$V_G = 10 \quad V_S = 0 \quad V_D = 0 \quad V_{SUB} = 0 \quad N_A = 2 \times 10^{16}\ cm^{-3}$

Figure 1-11: Cross-section of conventional isolation region structure with a plot of the surface potential versus the horizontal position. T_{ox} = 6500 Angstroms, x_j = 0.8 μm.

calculated surface potential of the semiconductor, in the corner regions of the thick field oxide. Instead of the barrier being centered under the gate, it is now located at the oxide corners. This can be understood by examining the two crosshatched regions which are bounded by the oxide/semiconductor interface, the depletion edge, and two electric field lines. At the planar region in the middle of the channel, this region is rectangular in shape, while the analogous region at the corner of the oxide is pie-shaped. Thus for equal interface areas and depletion widths, the pie-shaped region will contain more bound depletion charge than is needed to support the gate voltage; therefore the depletion width is less at the corner than at the middle of the channel. The depletion width is thinner because the depletion charge supported by the gate voltage is more spread out. Because the depletion width is smaller, there is less band bending and hence the potential at the corner is less as well. This results in the surface potential distribution shown in Figure 1-12. As the gate voltage increases from a low value, the potential at the corners increases much more slowly than in the middle of the channel.



$V_G = 18 \quad V_S = 0 \quad V_D = 0 \quad V_{SUB} = 0 \quad N_A = 2 \times 10^{16}\ cm^{-3}$

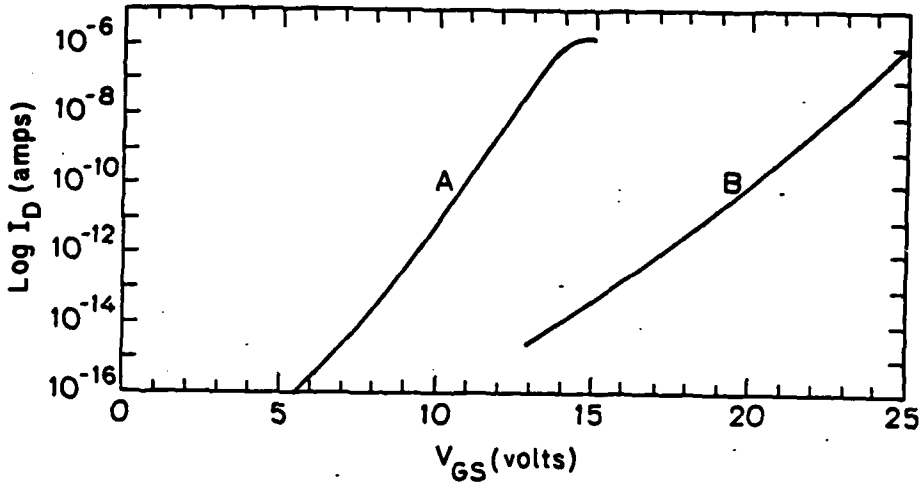
Figure 1-12: Cross-section of isolation region structure with the corner effect and a plot of the surface potential showing the new position of the barriers near the oxide corners. T_{ox} = 6500 Angstroms, x_j = 0.25 μm.

The two devices of Figures 1-11 and 1-12 have been biased in the simulations to produce the same drain current of 4pA/μm of channel width. Because of the corner effect, the gate voltage is 10 V in Figure 1-11 but is increased to 18 V for the device in Figure 1-12. The higher gate voltage has produced a strong inversion condition in the center region of Figure 1-12; the current is then limited by the potential barriers at the corner regions.

A second way of understanding the corner effect is to recognize that at the corner, the electric field lines diffuse and spread out as they penetrate into the semiconductor. Thus there is a weaker link of the potential in the semiconductor to the gate voltage, as shown by the plot of the potential. This viewpoint reveals that the corner effect is not limited to the semiconductor but also occurs in the oxide because of its shape. The electric field lines emanating from the gate begin spreading in the

oxide and continue to do so in the semiconductor. The spreading or fringing of the electric field lines and its effect on electrical characteristics, is similar to the narrow width effect seen in the shrinking of active devices.

The different characteristics of the corner device, which is essentially a modified concave MOSFET [11], allows the modeling of an isolation device by three devices whose channels are in series, two corner devices and a planar device. Because of the geometrical effects explained above, the corner device has a flatter subthreshold slope and a higher threshold voltage, and thereby controls the current flowing in the isolation device. Figure 1-13 is a plot of the calculated log(I_D) vs. V_{GS} curves for the devices depicted in Figures 1-11 and 1-12. The device with the corner effect clearly has better isolation due to the flatter subthreshold slope as well as the higher threshold voltage. (Note that the most useful definition of "threshold voltage" in these devices is probably the gate voltage necessary to induce a leakage or subthreshold current of some value --- perhaps 1 pA per micron of device width. Using this definition of threshold voltage, the corner effect increases it from 9 V to 17 V.) Thus for a given gate voltage, the device with the corner effect passes much less current than the device without.



A. NORMAL DEVICE
B. DEVICE WITH CORNER EFFECT

Figure 1-13: Calculated I--V curves for the devices of Figures 1-11 and 1-12. The device with the corner effect displays better isolation than the normal device without the corner effect.
V_{DS} = 5 V, V_{SUB} = 0 V.

The corner effect requires an applied gate voltage to exist and affect the device physics. Initially

when the potential in the semiconductor is unperturbed by the gate voltage, there is no spatial variation in the surface potential between the corner and central planar regions. Only when the gate voltage is increased and the semiconductor surface is perturbed by it, does the corner effect appear. Figure 1-14 shows several calculated plots of the surface potential along the Si/SiO_2 interface for several different voltages applied to the gate of the device shown in Figure 1-12. Notice that the corner effect does not emerge until the gate voltage begins to perturb the surface potential. As a result, a transistor with the corner effect goes through several stages of operation as the gate voltage is increased. At low gate voltages, the surface potential is only slightly affected by the gate and the transistor behaves in a conventional manner with the entire channel acting as a barrier to current injection from the source. The drain current then shows a $1/L$ dependence because the entire channel contributes to the potential barrier. As the gate voltage is increased the transistor operation enters a transition zone where the potential barrier is slightly larger at the oxide corners than at the central planar region. The planar region thus has a diminished effect on the current flow and transistors operated in this regime have a weak $1/L$ dependence. When the gate voltage is further increased, the transistor operates in a mode where the current flow is controlled only by the corners and is unaffected by the center region. This is because the potential barrier is much larger at the corners than in the middle of the channel. When the corner device dominates the parasitic transistor, the effective channel length of the parasitic transistor changes from the distance between the source and drain, to the distance along the curved portion of the oxide/semiconductor interface. As a result, transistors with the corner effect and different source to drain spacings, do not show the typical $1/L$ dependence in subthreshold current, but are approximately independent of L.

For the potential barrier to move from the center of the channel to the corner, the channel must exist around the corner of the oxide, and be controlled by the gate. This means not only the metallurgical boundary of the source, but also the portion of the depletion region controlled by the source, must lie above the corner for the isolation to be improved. Thus the junction depth is of crucial importance to the corner effect. The position of the potential barrier at the corner implies that the device can be shortened without degrading the isolation properties of the device. The cause of short channel effects, drain induced barrier lowering, is relatively ineffective due to the new location of the potential barrier. The drain voltage must affect the surface potential at the oxide corner near the source to alter the controlling potential barrier. If the electric field lines from the drain do reach the oxide corner, their effect is further reduced by the same geometrical arguments that limit the influence of the gate.

Another computer program was used to analyze the effect of drain biases on the device physics of

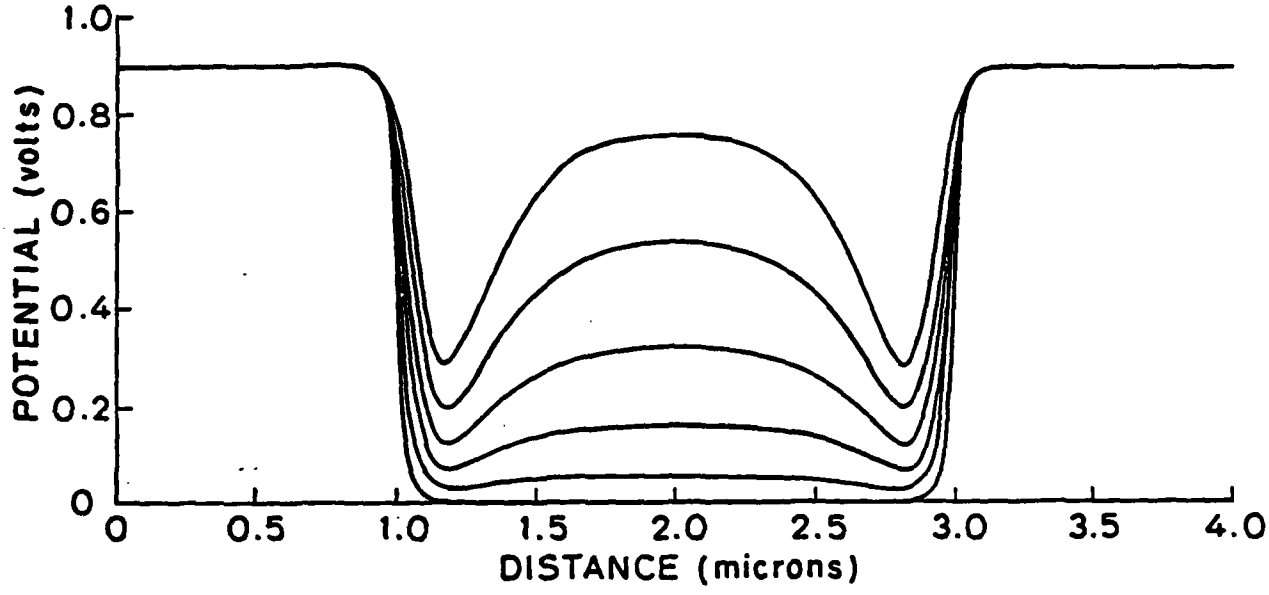


Figure 1-14: Plots of the surface potential of the transistor with the corner effect in Figure 1-12, illustrating the formation of the potential barriers at the corners with increasing gate voltage. $V_S = 0$ V, $V_D = 0$ V, $V_{SUB} = 0$ V, $V_G = -0.8, 2, 5, 8, 11, 14$ V.

the isolation transistor. The GEMINI program has limited usefulness for understanding structures with the corner effect and applied drain biases due to its treatment of inversion layers. The computer program PISCES solves Poisson's equation and the one carrier continuity equation in two dimensions, for structures with non-planar interfaces [12]. This enables PISCES to simulate parasitic transistors with the corner effect, in the subthreshold regime with appreciable drain biases, and also in the regime where the device is turned on. Figure 1-15 contains several surface potential plots of the device illustrated in Figure 1-12 for different drain biases. These plots illustrate that the potential barrier adjacent to the source is not affected by the drain potential.

The potential barrier adjacent to the drain, however, is modulated by the drain potential. At sufficiently high drain biases, the electric field from the drain supports a large amount of bound depletion charge around the adjacent oxide corner. This results in more band bending there, a reduction in the height of the potential barrier, and eventual elimination of the barrier adjacent to the drain. The removal of the drain potential barrier leaves only the potential barrier adjacent to the source providing the isolation. If the gate voltage has inverted the semiconductor in the middle of the channel, the reduction in the height of the drain barrier allows the pool of minority carriers to escape, which changes the channel into a state of deep depletion.

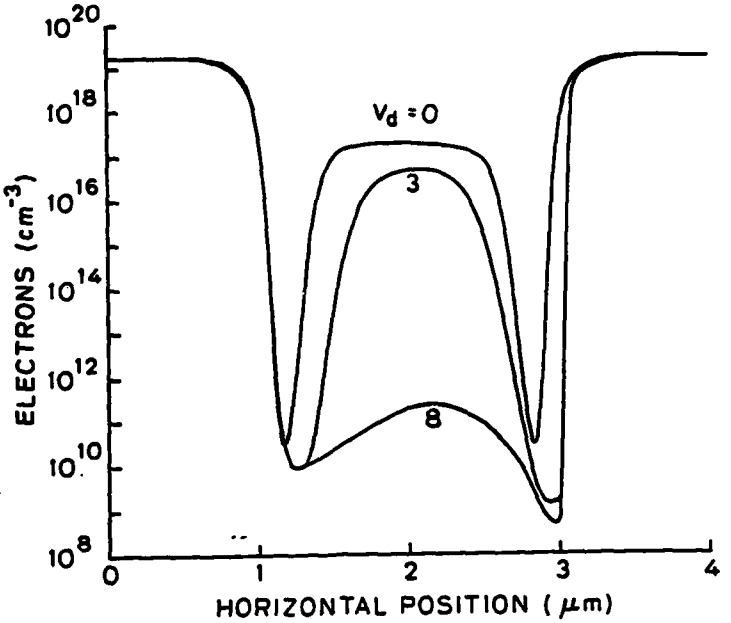


Figure 1-15: PISCES generated plots of the surface potential of a device with the corner effect showing the effect of drain bias. $V_G = 18$ V, $V_S = 0$ V, $V_{SUB} = 0$ V, $V_D = 0, 0.5, 3, 8$ V. $N_{SUB} = 2 \times 10^{16} cm^{-3}$.

The curvature of the oxide/semiconductor interface plays a major role in the corner effect. By varying the radius of the interface as in the devices of Figure 1-16, very large differences in electrical characteristics result, as seen in the plots of the calculated subthreshold currents in Figure 1-17 for those two devices. The gate voltage necessary for 1pA/μm of channel width increases from 11 V to 37 V. A normal planar device is the limit of a corner device with a very large radius. A device with a radius of zero, or a sharp corner, has a very large corner effect due to the difficulty the electric field experiences in reaching into the corner and the rapid increase in available depletion charge as the depletion width increases. Thus corner effect devices with sharper corners provide better isolation by having flatter subthreshold slopes and higher threshold voltages. The angle of the oxide corner also plays a role in determining the amount of the corner effect. The lower device of Figure 1-16 has a radius of zero and a right angle corner. As the angle increases, the electric field will be able to penetrate the corner better and the corner effect will be lessened. When the angle approaches 180° the corner effect will disappear.

A possible very small isolation structure resulting from the application of these principles is shown in Figure 1-18. The channel 'length' has been shortened to 0.2 μm and the oxide thickness increased to 0.95 μm. The additional solid lines in the figure are equipotential curves. The lower portion of

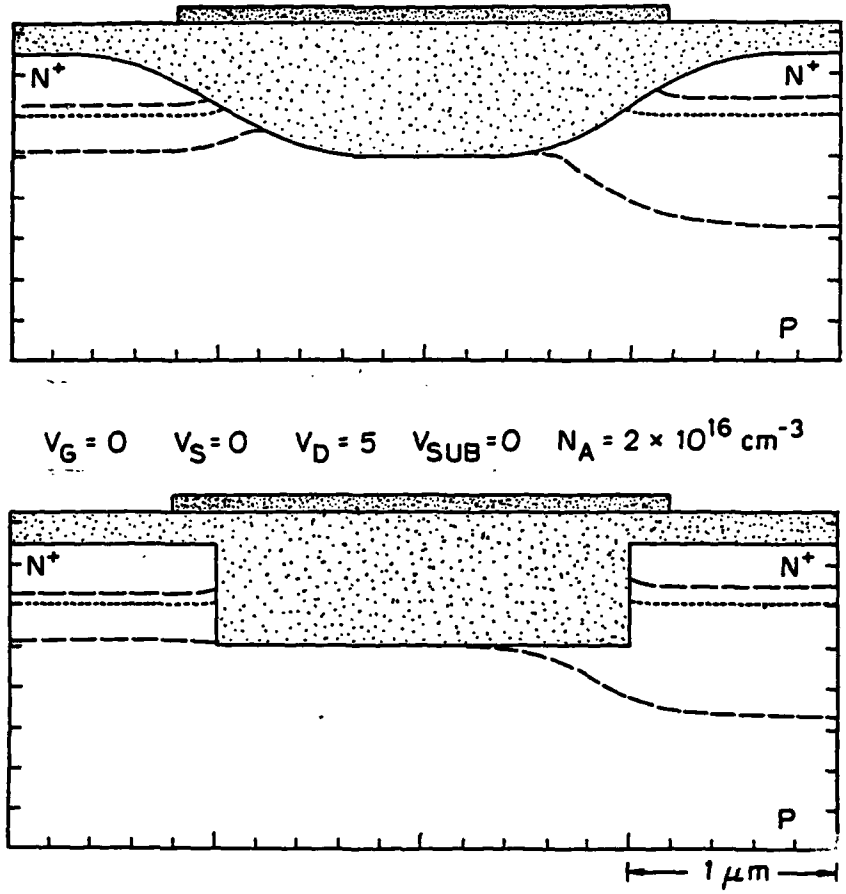


Figure 1-16: Cross-sections of isolation region structures with different interface curvatures. The top structure has a larger radius than the bottom structure. $V_{DS} = 5$ V, $V_{SUB} = 0$ V.

Figure 1-18 shows a plot of the calculated log(I_D) vs. V_{GS} curve for the device. This transistor has a flat subthreshold current curve because the gate has no control of the surface potential at the corner, which can be seen by the shape of the calculated equipotential curves. The drain controls the potential barrier. The drain current that flows is a function of the voltage on the drain, the distance from the drain to the corner, and the amount of the corner effect. Thus the current can be controlled by the depth of the oxide cut; the deeper the cut --- the less current. This is because the depth of the cut determines which equipotential curve intersects the lower left corner of the oxide, and hence the potential barrier height. A structure such as this could have considerable use in the isolation between adjacent diffused lines in a chip, by allowing a much closer spacing of them.

The addition of a substrate bias enhances the corner effect. The additional gate voltage required for the extra band bending changes the surface potential less at the corner than in the planar region and hence heightens the corner effect. Figure 1-19 shows the smaller increase of depletion width at

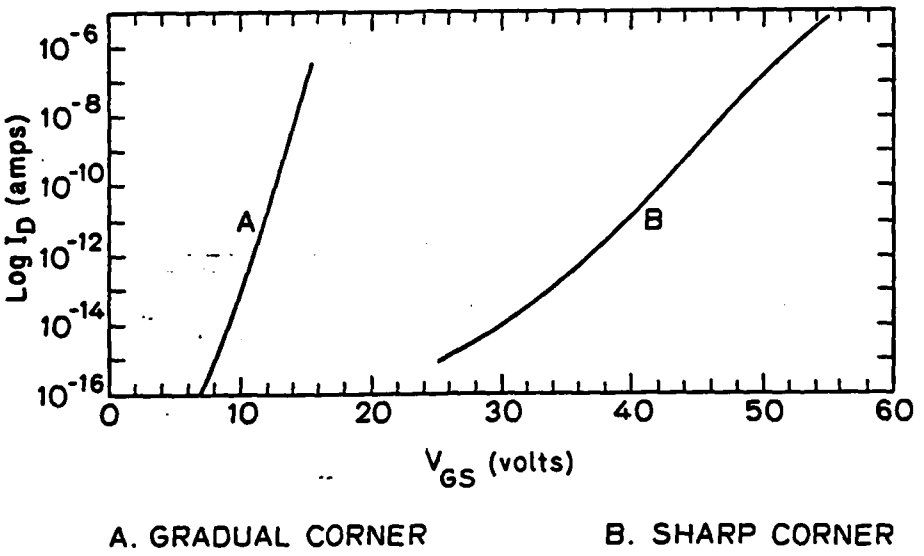


Figure 1-17: Calculated I--V curves for the devices of Figure 1-16. The device with the sharp corner displays better isolation than the device with the gradual corner.

the corner for an applied substrate bias of -2 V and the greater shift obtained in the calculated log(I_D) vs. V_{GS} curves for devices with the corner effect. The subthreshold curves of the device with the corner effect (curves B and D) shift 25 V while the curves of the device without (A and C) shift 13 V.

Changes in the doping of the field transistor's channel affect the corner effect in different ways, so that the overall change in electrical characteristics will depend on the configuration of the particular structure. Heavier doping results in the depletion edges of the source and drain being pulled up and thereby producing a greater corner effect by including more of the corner in the channel. Heavier doping also results in a thinner depletion region around the corner which reduces the two-dimensional aspect of the corner in the semiconductor and lessens the corner effect. From a practical point of view, only a small range of substrate doping is of interest for isolation structures, since to minimize junction capacitances, the smallest doping consistent with the required threshold voltage would be used. The transistors in this report all have uniformly doped substrates, but the corner effect also applies to transistors with localized field implants. If the device is fabricated in such a way that the field implant extends out to the corners, the corner effect will still dominate the device physics. Simulations of isolation devices with field implants on lightly doped substrates have shown that dopant concentration can be less at the corners than in the middle of the transistor, and yet the corner effect can still enhance the isolation. This is because the geometrical weakening of the linkage between the gate and the substrate outweighs the lighter doping in the corner.

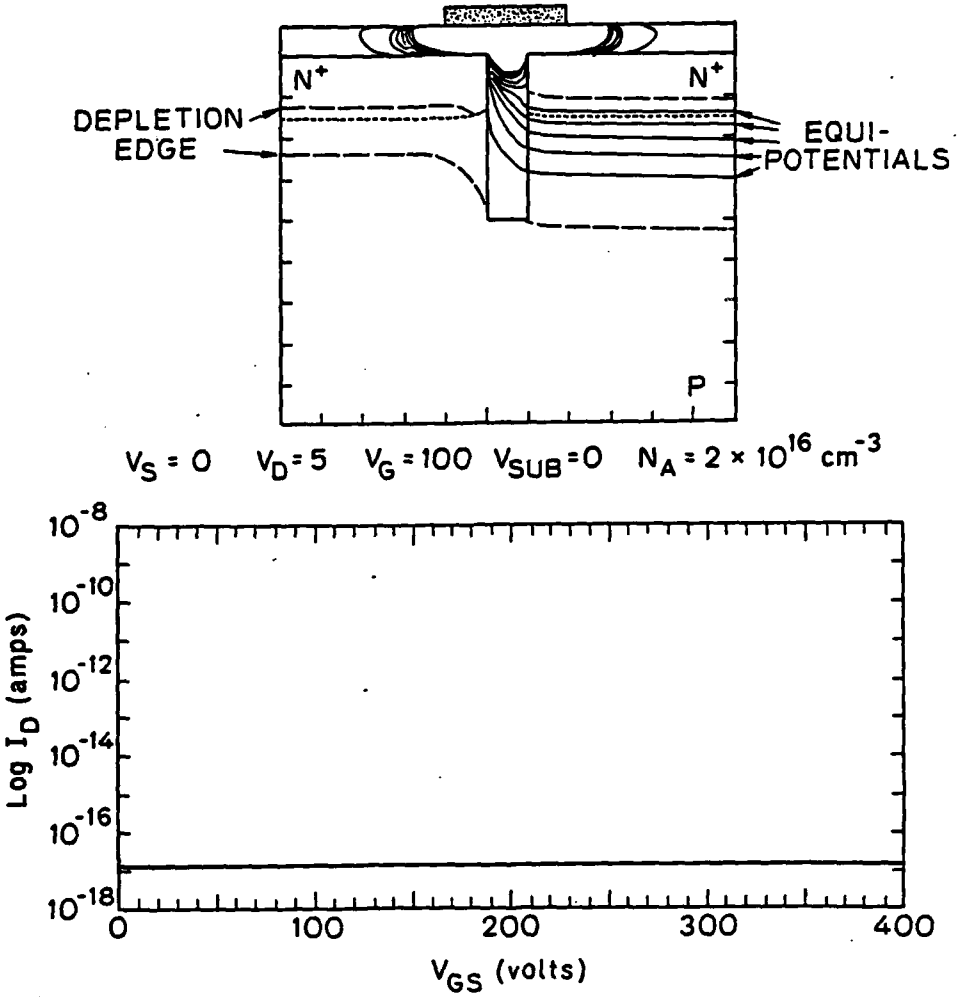


Figure 1-18: Cross-section of small isolation region transistor with its calculated I--V characteristics. The gate has no control of the drain current.

Analytical Development

The previous section has demonstrated with the aid of specific computer simulations, the basic ideas which can be used in optimizing isolation region structures. When actually optimizing these structures, however, it would be a great value to have a reasonably simple analytic expression which relates the electrical properties of the isolation structure (threshold voltage, subthreshold slope, etc.) to the physical properties of the structure (trench depth, oxide thickness, corner radius, etc.). Such an analytical relationship would be faster and more powerful than the computer simulations and would also aid in estimating the sensitivity of the electrical properties to structural changes as well.

A first order analysis of the corner effect can be accomplished by considering the physics of the

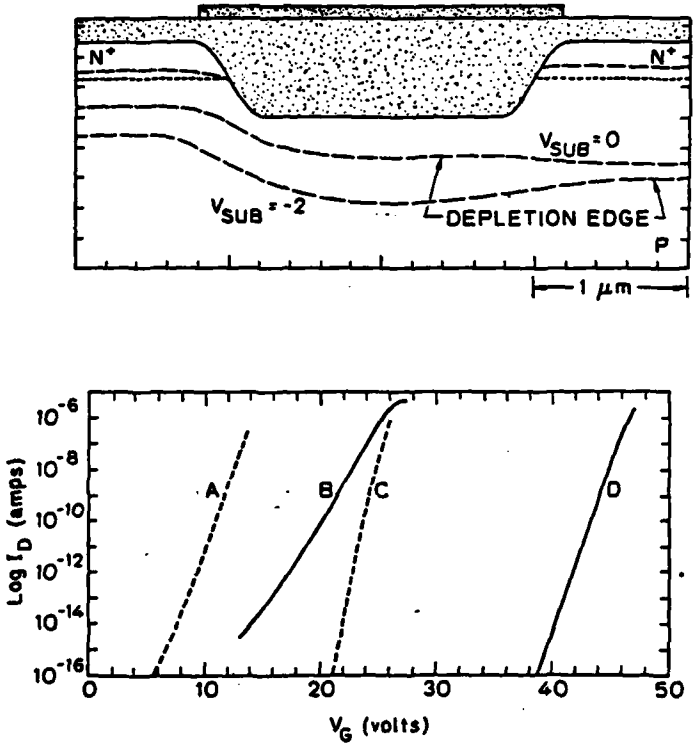


Figure 1-19: Effects of substrate bias. The cross-section of a isolation region device with the corner effect shows the smaller increase in the depletion width at the corner than at the center planar section. A transistor with the corner effect shows a larger shift in the calculated I--V curves with an applied substrate bias than one without.

corner device and assuming the corner device dominates the parasitic transistor. This has been done in two separate parts [6]. The first part determined the capacitance of the oxide structure with conformal mapping. This produces the variation of the capacitance along the oxide/semiconductor interface in the corner region with the geometry of the oxide. The second portion was the derivation of the MOS equations in the semiconductor corner region. This was done by solving the one-dimensional equations in cylindrical coordinates. Then the two parts were brought together for the complete analysis of the corner effect.

The details of the analytic development are contained in [6]. We show here only an example of the

results. Figure 1-20 shows a plot of the parasitic transistor inverse subthreshold slope n versus r for $N_{SUB} = 2 \times 10^{16}$ cm^{-3}, $T = 6500$ Angstroms, and $\varphi_S = 0.5$V. The plot shows a dramatic increase in n as the radius decreases. This translates into greatly improved isolation because the semiconductor is less influenced by the gate for very small r. Also shown in Figure 1-20 are several discrete points that correspond to subthreshold slope data acquired from GEMINI simulations. The point at the far right hand side of the plot is from the one-dimensional analysis, or a radius of infinity. The point for $r = 0$ has a finite slope factor instead of the infinite value predicted by the analytical development. This is due to simplifying assumptions in the analytic development.

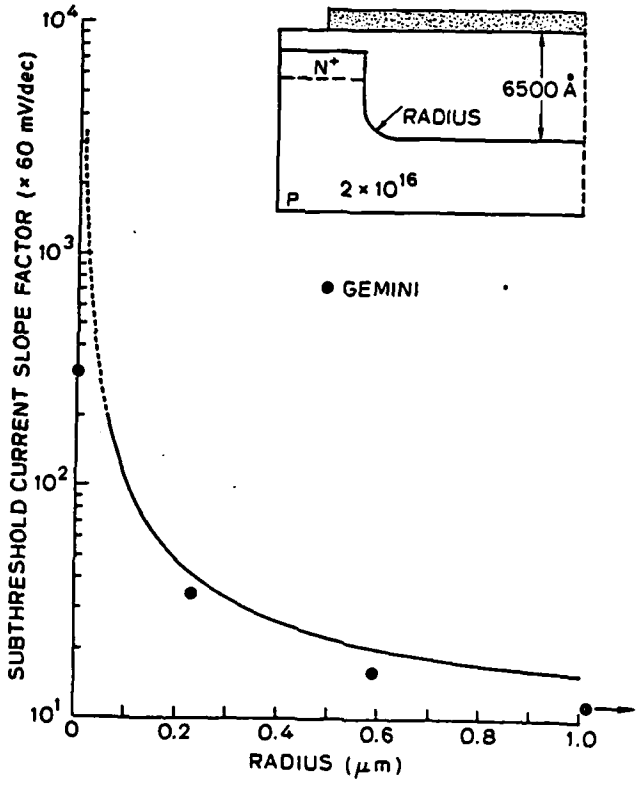


Figure 1-20: Plot of the subthreshold slope factor versus the interface radius. The discrete points are from GEMINI simulations, with the one on the far right hand side from standard one dimensional analysis. A device with a small interface radius will have a flatter subthreshold slope and hence better isolation.

Figure 1-20 reveals a direct link between an electrical parameter, the subthreshold slope, and a structural parameter, the corner radius. It is clear that subthreshold slope is sensitive to the value of the corner radius and becomes very sensitive for values below 0.25 μm. Thus in designing a process for the fabrication of isolation structures for VLSI, one would want a small corner radius in order to provide good isolation. This influences the choice of how a trench is etched in the silicon substrate and also how it is filled. If the process depends on the sharp corners to provide the necessary isolation, great care must be taken to ensure that the variations in the radius are sufficiently small to minimize leakage currents in worst case processing variations. The analysis can be expanded to provide an equation for the subthreshold current as a function of the gate voltage and structural parameters [6].

Smaller radii and sharper angles improve the isolation according to the device physics of the structure's geometry. That geometry, however, may lead to an increased number of crystal defects because of stresses due to the fabrication [5]. These defects can cause excessive leakage currents and hence alter the electrical characteristics of the device. A fabrication process must consider not only the geometry of the isolation device, but also the material qualities that result from that structure, in arriving at an optimal structure.

Experimental Results

Devices have been fabricated to verify the corner effect experimentally. Because of the very low current levels of the subthreshold regime, the devices were designed with large channel widths of 500 μm and 2820 μm. Channel lengths varied from 1.25 to 40 μm on the mask. In initial fabrication runs, the devices were made on <110> oriented silicon wafers with a KOH etch to produce vertical side wall grooves that were later oxidized to form the field oxide isolation devices. That orientation of silicon was chosen to obtain sharp right angle corners in the grooves. The bottom surfaces of the etched grooves were not as smooth as desired however, and to avoid such problems, the devices described here were made on <100> wafers with plasma etching of the silicon to produce similar structures. Arsenic was used for the source and drain to ensure shallow junctions above the oxide/semiconductor interface. The relative position of the junction depth and oxide interface was varied by changing the junction drive-in time, to produce structures with and without corner effects. Different oxide/semiconductor interface radii, r, were produced by controlling the silicon etching and subsequent oxidation.

The transistors were fabricated on p-type 6 Ω-cm wafers. A portion of each wafer was implanted with boron (100 keV, 9×10^{12} cm^{-2}) to produce other transistors with a heavier substrate doping.

Subsequent high temperature processing spread this implant out enough to consider the doping to be uniform. Figure 1-21 displays some cross sections of a test transistor during the processing sequence. Arsenic was implanted (120 keV, 1×10^{15} cm^{-2}) in the source, drain, and gate regions. A pad oxide was then grown and silicon nitride deposited. Following patterning using photoresist, the exposed Si_3N_4 and SiO_2 were removed from the regions in which the isolation regions were to be formed. This was followed by the etching of the silicon substrate, still using the same patterned photoresist as a mask. By etching through the arsenic layer, the source and drain were defined. The gate region was locally oxidized using the Si_3N_4 as a mask over the source and drain. The remainder of the processing was a standard polysilicon gate NMOS process. The resulting test structures are shown in Figure 1-22.

Three different interface radii were fabricated to investigate varying amounts of the corner effect. The structure with the largest oxide/semiconductor interface radius was fabricated by isotropically etching a trench and then thermally growing a 6400 Angstroms oxide at 950°C in H_2O. Plasma etching with SF_6 was used to produce curved sidewalls whose radii were increased further by the oxidation. Figure 1-23 contains an SEM cross-section of this structure. An intermediate radius structure was fabricated by anisotropically etching the trench and then growing a 6400 Angstroms oxide. The use of Freon 115 (C_2ClF_5) for the plasma etching produced vertical sidewalls with relatively sharp corners. The subsequent oxidation substantially increased the radii of the oxide corners because of the 2D oxidation process in the corner regions. Anisotropic etching of the trench with Freon 115, followed by the growth of 3000 Angstroms of oxide and then the deposition of 3400 Angstroms more resulted in the third device structure which had the smallest interface radius. An additional inert ambient anneal was done for these structures to compensate for the shorter oxidation time. Figure 1-24 contains an SEM cross-section of this structure. The radii of the corners produced by the Freon 115 did not increase as much because of the thinner thermal oxide. The radius of the interface is substantially smaller in Figure 1-24 than in Figure 1-23, 0.57 μm compared to 1.00 μm. The corner radius of Figure 1-24, however, is significantly larger than the radius produced by the Freon 115 etching because of the 2D effects of the thermal oxidation. It should also be noted that in all of these structures the polysilicon gate lies below the original silicon surface since the etched trenches were not completely refilled by the oxidation and/or SiO_2 deposition processes. More ideal isolation region structures (similar to Figure 1-12) could be obtained with a more advanced technology which provided complete refilling and planarization.

Figure 1-25 shows the subthreshold characteristics of four typical devices. All have channel widths of 500 μm and channel lengths of 7.5 μm on the mask. The oxide thickness is 6400 Angstroms and

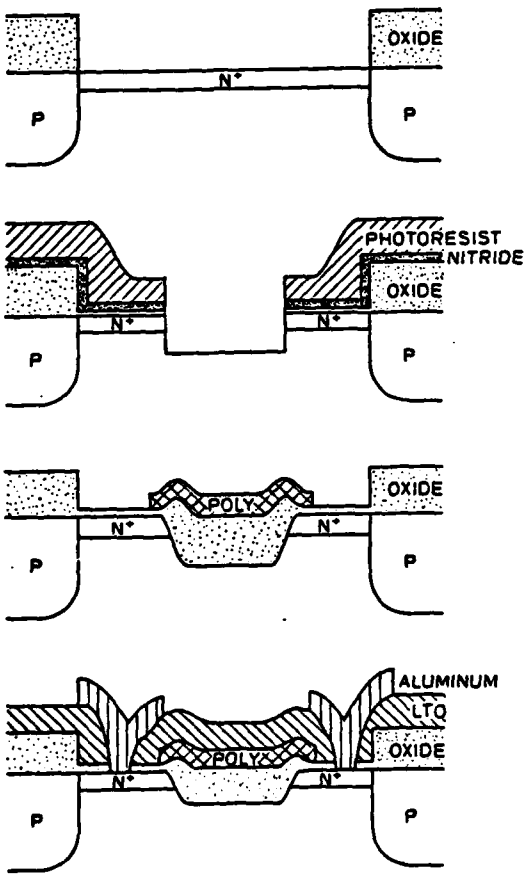


Figure 1-21: Cross sections of a test transistor during the fabrication process. Top: after the arsenic has been implanted in the source, gate, and drain regions. Upper middle: after the etching of the silicon in the gate region. Lower middle: after the polysilicon has been deposited and defined. Bottom: The completed test transistor.

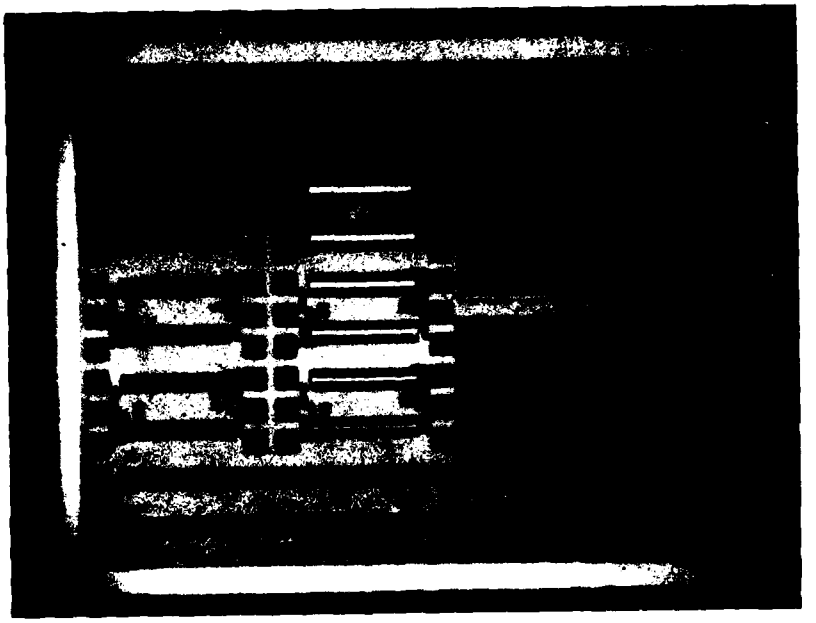


Figure 1-22: Microphotograph of experimental test structures.

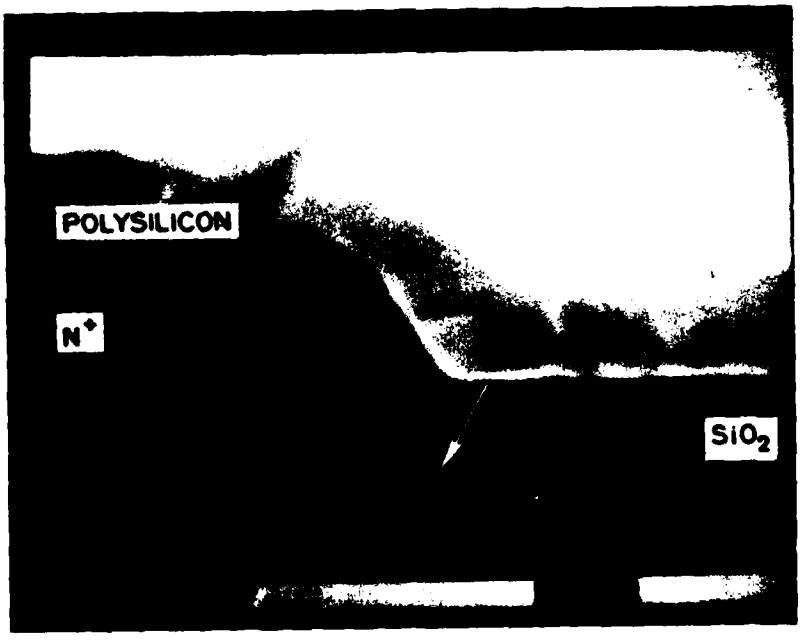


Figure 1-23: SEM cross-section of isolation structure with the largest fabricated interface radius. $r = 1.00\ \mu m$.

the substrate was implanted with boron to increase the surface doping to $\approx 1.3 \times 10^{16}$ cm^{-3}. They

Figure 1-24: SEM cross-section of isolation structure with the smallest fabricated interface radius. $r = 0.57\ \mu m$.

were measured with $V_{DS} = 0.05$ V and $V_{SUB} = 0.0$ V. Curve A is from a transistor whose source/drain junctions have been driven in below the oxide corner and thus obeys simple one dimensional MOS equations. Its measured subthreshold slope is 0.56 V/dec. Curve B corresponds to the structure of Figure 1-23 which has the largest corner radius of the fabricated devices. It displays a slightly flatter subthreshold slope, 0.74 V/dec, and higher threshold voltage compared to A. The transistor whose trench had been etched with Freon 115 and had all the field oxide thermally grown, has the subthreshold characteristics of curve C. Its interface radius is smaller and the resulting subthreshold curve is flatter than the previous two curves, 0.80 V/dec. The fourth subthreshold curve, labeled D, corresponds to the structure of Figure 1-24. This device has the sharpest corner of all the fabricated devices. As a result the subthreshold curve is much flatter than the previous curves and the isolation is significantly improved. The subtheshold slope of Curve D is 1.10 V/dec. Between devices A and D, there is about a factor of two improvement in isolation where isolation is defined as the gate voltage needed to produce 1 pA/μm of channel width of leakage current.

The effects of a substrate bias are shown in Fig .re 1-26. The log(I_D) vs. V_{GS} curves of two different devices are shown, one with the corner effect and one without. The structures were fabricated on a boron implanted substrate and have channel lengths of 2.5 μm and a widths of 500 μm, $V_{DS} = 0.05$

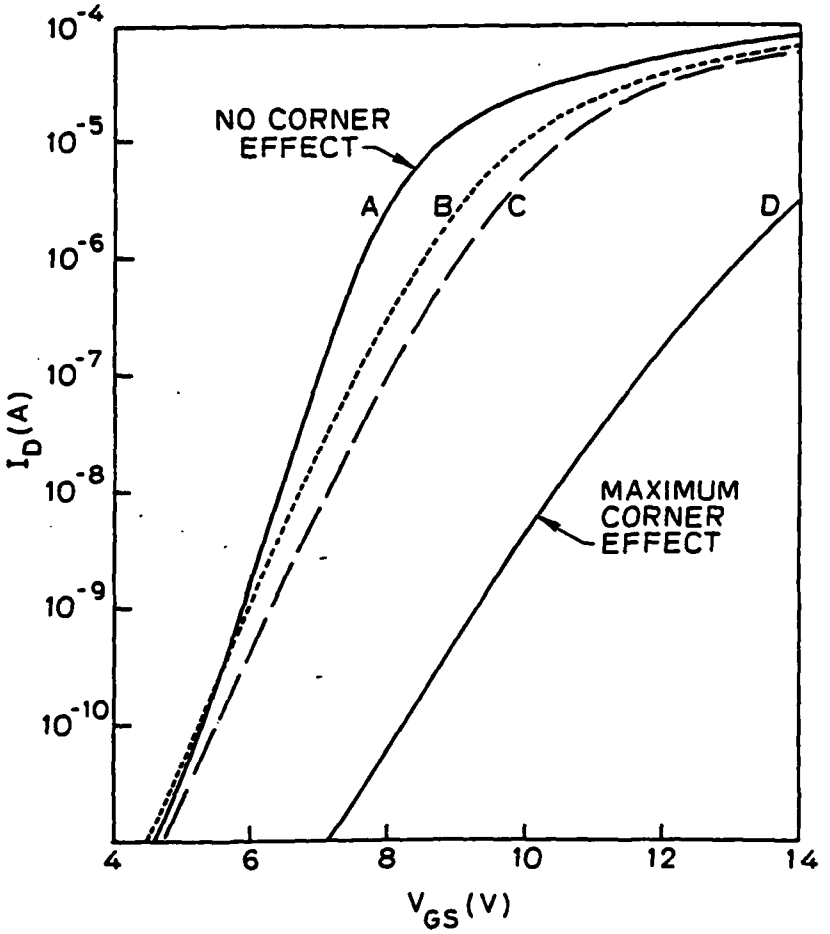


Figure 1-25: Plot of measured I--V characteristics of four devices with varying amounts of the corner effect. Curve A is from a device with no corner effect. Curves B, C, and D are from devices with decreasing interface radii. $V_{SUB} = 0.0$ V, $V_{DS} = 0.05$ V, channel length is 7.5 μm, width is 500 μm. $N_{SUB} \approx 1.3 \times 10^{16}$cm^{-3}.

V. Curves A and B are from a transistor without the corner effect, and a substrate bias of 0.0 and -0.5 V respectively. Curves C and D are from a device with the smallest fabricated corner radius (Figure 1-24), and a substrate bias of 0.0 and -0.5 V respectively. The shift between curves A and B is 3.4 V at a current level of 500 pA, while the shift between curves C and D is 6.0 V. The characteristics of the corner region produce a larger shift in the threshold voltage for a given substrate bias, and hence improved isolation. The subthreshold slopes also steepen for both cases with the addition of the bias, as expected.

The SEMs of Figures 1-23 and 1-24 can be used to create GEMINI simulations with the same

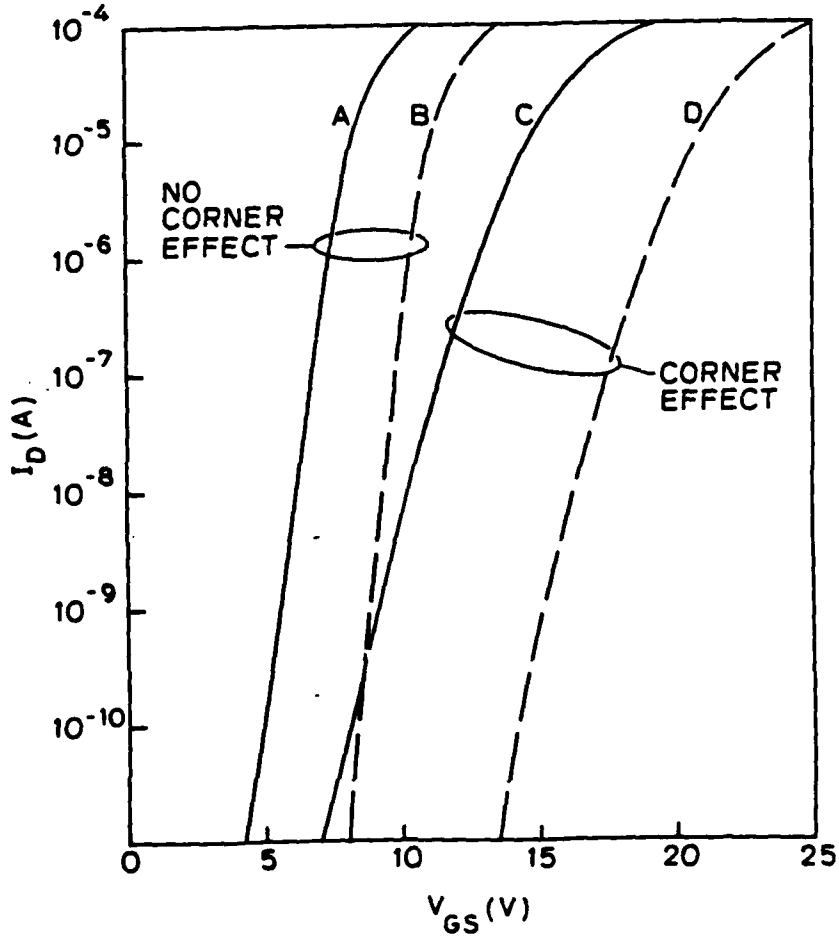


Figure 1-26: Plot of measured I-V characteristics of two devices displaying the effect of substrate bias. Curve A: no corner effect, $V_{SUB} = 0.0$ V; Curve B: $V_{SUB} = -0.5$ V. Curve C: with corner effect, $V_{SUB} = 0.0$ V; Curve D: $V_{SUB} = -0.5$ V. Channel length is 2.5 μm, width is 500 μm. There is a larger shift in the curves due to applied substrate bias in the device with the corner effect. $N_{SUB} \approx 1.3 \times 10^{16} cm^{-3}$.

physical structure. The structure can be simulated over a range of gate voltages to create a subthreshold curve. The simulated curves agree with the experimentally measured curves, and as can be seen in Figure 1-20, the GEMINI simulations agree with the analytic model. It should be noted that it is difficult to ascertain the exact value of the interface radius from the SEMs and GEMINI simulations, which hinders efforts to make exact comparisons.

Figure 1-27 displays the insensitivity of a transistor with the corner effect to short channel effects. The subthreshold curves of two devices, with and without the corner effect, are shown for drain

voltages of 0.5 and 5.0 V. The structures have channel lengths of 2.5 μm and widths of 500 μm. The substrate is uniformly doped with a resistivity of 6 Ω-cm, and the substrate bias is 0.0 V. Because of the more lightly doped substrate, the threshold voltages are much smaller than in the previous two figures. Curves A and B are for a device with deep junctions that obeys the 1D MOS equations with drain voltages of 0.5 and 5.0 V respectively. Curves C and D are for a device with the corner effect (Figure 1-24), and drain voltages of 0.5 and 5.0 V respectively. There is a much larger shift with the increased drain voltage for the normal device than for the device with the corner effect. This is due to the isolation of the corner effect transistor's potential barrier from the drain voltage. The shifting of the barrier from the center of the channel to the source makes drain induced barrier lowering (DIBL) much less important, as was explained earlier and illustrated in Figure 1-15.

To further illustrate the corner effect's immunity to short channel effects, consider Figure 1-28. The drain current is plotted versus the drain voltage for the same two devices that are used in Figure 1-27. The gate voltages are held constant at values that put each transistor in the subthreshold regime. For an ideal long channel 1D device, theory predicts I_D proportional to $1-\exp(-qV_{DS}/kT)$. The curve for the structure without the corner effect, A; shows this rise in current for small values of V_D. However, as the drain voltage continues to increase, the current begins to rise at an increasing rate. This is indicative of DIBL as the increasing V_D begins to reduce the potential barrier height. Curve B, of the structure with the corner effect, does not show this superlinear increase in current, but instead I_D levels off as V_D is increased. Clearly, the corner effect can significantly improve the isolation provided by parasistic transistors with small channel lengths.

1.2.1.3 Summary of Results

The availability today of controlled anisotropic etching makes it feasible to consider trench-like structures where the isolation oxide extends significantly deeper into the silicon than the source/drain junctions. When this is done, a substantial improvement in isolation is obtained due to geometrical arguments. The corner effect provides flatter subthreshold slopes and higher threshold voltages, and is strongly dependent on the junction depth and the interface radius of curvature. A mathematical analysis of the physics of the corner effect results in an equation relating the subthreshold slope and the radius of the interface. That strong dependence of the corner effect on the radius was verified by the testing of several test transistors with different radii. These measurements also demonstrated the improved isolation properties with substrate bias and drain voltage.

With this better understanding of the device physics of isolation transistors, some observations can

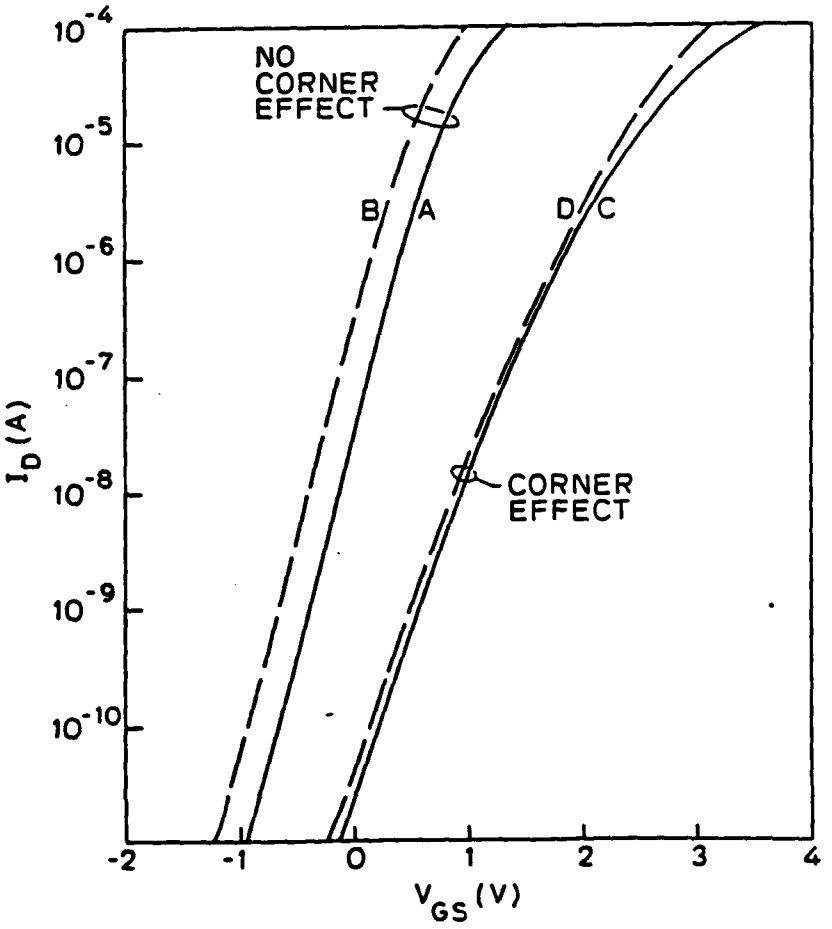


Figure 1-27: Plot of measured I--V characteristics of two devices displaying the effect of drain voltage. Curve A: no corner effect, $V_{DS} = 0.5$ V; Curve B: $V_{DS} = 5.0$ V. Curve C: with corner effect, $V_{DS} = 0.5$ V; Curve D: $V_{DS} = 5.0$ V. Channel length is 2.5 μm, width is 500 μm. There is a smaller shift in the curves due to the applied drain voltage in the device with the corner effect. $N_{SUB} = 1.5 \times 10^{15}$cm^{-3}.

be made about the various new fabrication techniques. Isolation that is made by etching away the field oxide in the active device regions [14], or by selectively oxidizing a deposited polysilicon layer into the field oxide [10], will not demonstrate the two-dimensional corner effect described in this paper because the Si/SiO_2 interface is planar and the oxide is above the source/drains. In addition to not realizing the better isolation due to the corner, short channel effects will remain a major problem. Other isolation techniques that bury the oxide in a trench-like structure, can take advantage of the better isolation available to it by adjusting the relative positions of the oxide interface and the source/drain junction depths. In addition to improved immunity to short channel effects, these

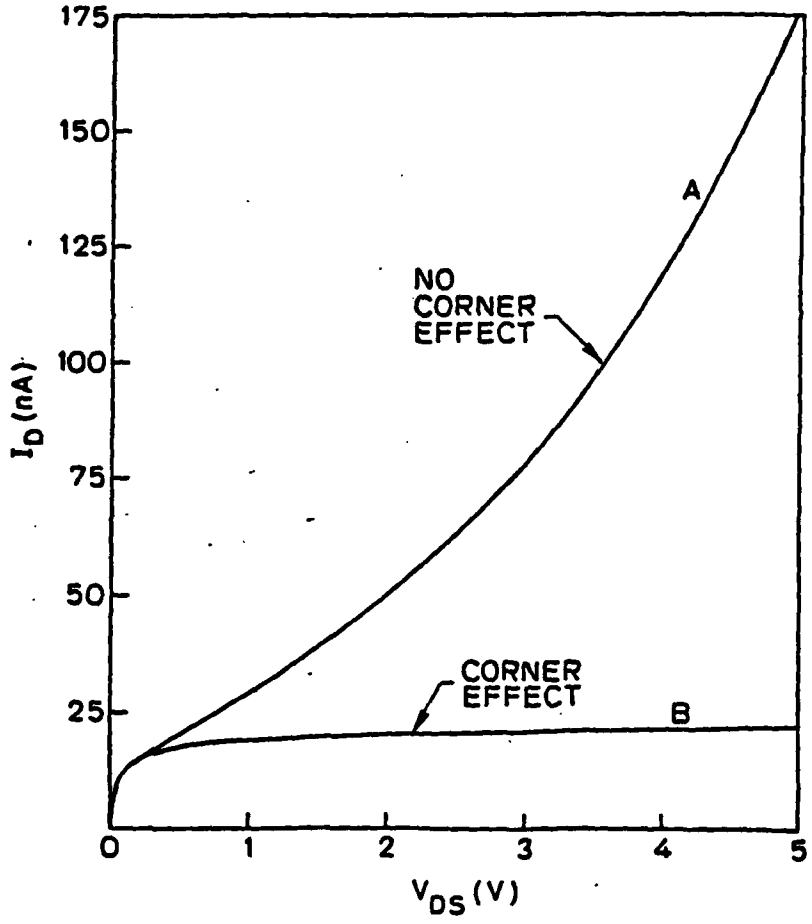


Figure 1-28: Plot of the drain current versus the drain voltage with a constant gate voltage. Curve A is from a device with no corner effect and V_G = -0.06 V. Curve B is from a device with the corner effect and V_G = 1.07 V. Channel length is 2.5 μm, width is 500 μm. The device with the corner effect does not experience drain induced barrier lowering. $N_{SUB} = 1.5 \times 10^{15} cm^{-3}$.

techniques provide a planar top surface for easier subsequent processing. However, in addition to optimizing electrical characteristics through a careful choice of isolation region geometry, other effects such as stress, defect production in the substrate, and charges on the sidewalls should also be considered [3]. This paper has attempted to point out that with these new techniques, both device physics and processing techniques can point toward the same goal. Burying the oxide and sharpened oxide corners means improved isolation and more compact VLSI layouts.

1.2.1.4 References

1. J.A. Appels, E. Kooi, M.M. Paffen, J.J.H. Schatorge, W.H.C.G. Verkuylen. "Local Oxidation of Silicon and its Application in Semiconductor Device Technology." *Phillips Research Reports 25* (1970), 118-132.

2. J. Y. Chen, R. C. Henderson, J. T. Hall, and E. W. Yee. A Fully Recessed Field Isolation Using Photo-CVD Oxide. IEDM Technical Digest, IEEE, December, 1982, pp. 233-236.

3. S. Y. Chaing, K. M. Cham, D. W. Wenocur, A. Hui, and R. D. Rung. "Trench Isolation Technology for MOS Applications." *VLSI Science and Technology* (October 1982), 339-346.

4. K. Y. Chiu, R. Fang, J. Lin, J. L. Moll, C. Lage, S. Angelos, R. Tillman. The SWAMI -- A Defect Free and Near-zero Bird's-beak Local Oxidation Process and its Application in VLSI Technology. IEDM Technical Digest, IEEE, December, 1982, pp. 224-227.

5. R. C. Y. Fang, K. Y. Chiu, and J. L. Moll. "Defect Characteristics and Generation Mechanism in a Bird Beak Free Structure by Sidewall Masked Technique." *Journal of the Electrochemical Society 130* (January 1983), 190-196.

6. S. Goodwin. Isolation Structures for VLSI -- Device Physics and Electrical Characteristics of Deep Groove Structures. Tech. Rept. TR # G725, Stanford Electronics Laboratories, January, 1984.

7. J. A. Greenfield and R. W. Dutton. "Nonplanar VLSI Device Analysis Using the Solution of Poisson's Equation." *IEEE Trans. Electron Devices ED-27* (August 1980), 1520-1532.

8. J. Hui, T. Chiu, S. Wong, and W. G. Oldham. "Sealed-Interface Local Oxidation Technology." *IEEE Trans. Electron Devices ED-29* (April 1982), 561-567.

9. K. Kurosawa, T. Shibata, and H. Iizuka. A New Bird's-beak Free Field Isolation Technology for VLSI Devices. IEDM Technical Digest, IEEE, December, 1982, pp. 384-387.

10. N. Matsukawa, H. Nozawa, J. Matsunaga, S. Kohyama. "Selective Polysilicon Oxidation for VLSI Isolation." *IEEE Trans. Electron Devices ED-29* (April 1982), 561-567.

11. K. Natori, I. Sasaki, and Fujio Masuoka. "An Analysis of the Concave MOSFET." *IEEE Trans. Electron Devices ED-25* (April 1978), 448-456.

12. C. H. Price. Two-dimensional Numerical Simulation of Semiconductor Devices. Tech. Rept. TR , Stanford Electronics Laboratories, May, 1982.

13. R. D. Rung, H. Momose, and Y. Nagakubo. Deep Trench Isolation CMOS Devices. IEDM Technical Digest, IEEE, December, 1982, pp. 237-240.

14. K. L. Wang, S. A. Saller, W. R. Hunter, P. K. Chatterjee, and P. Yang. "Direct Moat Isolation for VLSI." *IEEE Trans. Electron Devices ED-29* (April 1982), 541-547.

1.2.1.5 Recent JSEP Publications

1. S. H. Goodwin and J. D. Plummer. Trench Isolation Technology and Device Physics. VLSI Symposium, IEEE, September, 1983.

2. S. Goodwin. Isolation Structures for VLSI -- Device Physics and Electrical Characteristics of Deep Groove Structures. Tech. Rept. TR # G725, Stanford Electronics Laboratories, January, 1984.

3. S. H. Goodwin and J. D. Plummer. "Electrical Performance and Physics of Isolation Region Structures for VLSI." *IEEE Trans. on Electron Devices ED-31* (July 1984).

1.2.2 Alternative Gate Dielectrics for Submicron MOS VLSI

Investigators: M. M. Moslehi and K. C. Saraswat

1.2.2.1 Scientific Objective

Due to the continuing growth in the integration density of integrated circuits and the technological and reliability problems with silicon dioxide in the very thin regime (< 100 angstroms), there is a demand for new higher quality ultrathin insulators to replace silicon dioxide in highly scaled down VLSI IGFETs and memory devices such as DRAM and EEPROM. Thermal nitridation of *Si* and thin SiO_2 has been investigated in the past few years and appears to be an alternative to the oxidation process to grow good quality films in the very thin regime (< 100 angstrom).

Most of the recent work on thermal nitridation has been on technological issues such as composition, growth kinetics, oxidation resistance, and interactions with impurity diffusion [1, 17, 14, 4, 3, 11].

In the last report of this program, we reported a new technique to thermally nitride *Si* and SiO_2 in a cold-wall rf-heated reactor in an ammonia gas ambient. Growth kinetics of the nitride and nitroxide films was studied in the temperature range of 950 to 1200°*C* [14]. The physical properties of these films were characterized by auger electron spectrometry, Rutherford back scattering, and etch rate measurements [14]. Some electrical characterization was done by the capacitance-voltage measurement technique [13]. In a few cases devices made with nitroxide and nitride have been electrically characterized [7, 8, 13]. However, most of the work in the past has been on nitrided oxide. Nitridation of oxide results in the exchange reaction of nitridation species with oxide at the surface and interface regions and to a lesser extent in the bulk region. It has been reported that the generation of radiation-induced interface states in MOS devices is eliminated after proper high temperature nitridation of oxide [15]. This may be attributed to structural changes in the strained region of the oxide after nitridation in ammonia. We have observed [13], as Ito et al [9] have also

reported, that the breakdown characteristics of MOS structures can be improved by annealing the SiO_2 films in ammonia gas at high temperatures. The effects of nitridation of SiO_2 in ammonia on electron trapping has been investigated [12, 2] and it has been reported that ammonia nitridation results in a significant increase in electron trapping. However, the data presented so far have not been sufficient to draw firm conclusions regarding trapping in nitroxide insulators. Moreover, effects of annealing of nitroxide insulators in nitrogen, oxygen, or argon ambients on trapping characteristics should be studied more in detail.

Thermal nitride films can be grown by high temperature nitridation of silicon in pure ammonia [14], ammonia plasma [16, 10], or nitrogen-hydrogen plasma [6]. Ito et. al. have fabricated IGFETs with thermal nitride gate insulators showing good breakdown characteristics and high transconductance [7, 10, 8]. However, a more detailed electrical characterization of thermal nitride films including trapping has not been reported in the past. In this report the results of a study on conduction and trapping in thermal nitride gate insulators is presented. Cross-sectional TEM has been used to study the structure of thermal nitrides and their interface with the silicon substrate.

1.2.2.2 Progress

Experimental Procedure

MIS devices with thin oxide, nitroxide, and nitride gate insulators were fabricated with aluminum gate electrodes on n- and p-type *Si* substrates. The SiO_2 used in this work was grown to a thickness of about 100 angstroms in a furnace in oxygen at 900 °C. All thermal nitridations were performed in pure ammonia in a cold-wall RF-heated reactor described elsewhere [13]. Nitridations of *Si* and SiO_2 were performed at temperatures from 950 °C up to 1230 °C for times ranging from 30 minutes to 4 hours. The gate areas were 2.01×10^{-2}, 5.03×10^{-3}, 1.26×10^{-3}, 3.14×10^{-4}, and 7.85×10^{-5} cm^2. The gate electrode was Al-(1%)Si deposited in a flash evaporator.

Results and Discussion

Figure 1-29 illustrates the conduction characteristics of an MIS device with 64 angstroms of thermal nitride grown at 1230 °C for 4 hours on n-type (100) silicon with a resistivity of 0.5 *ohm.cm.* at 1230 °C for 4 hours and a gate area of 7.85×10^{-5} cm^2. Fowler-Nordheim (F-N) behavior can be observed over about six decades of current. At very high current levels bulk effects on conductivity become important resulting in deviation from Fowler-Nordheim behavior. The F-N parameters can be obtained from a comparison of the experimental data with the F-N expression $J = a.E^2 \exp(-b / E)$.

It is well known that for thick SiO_2 gate insulators the current density at a given field is independent

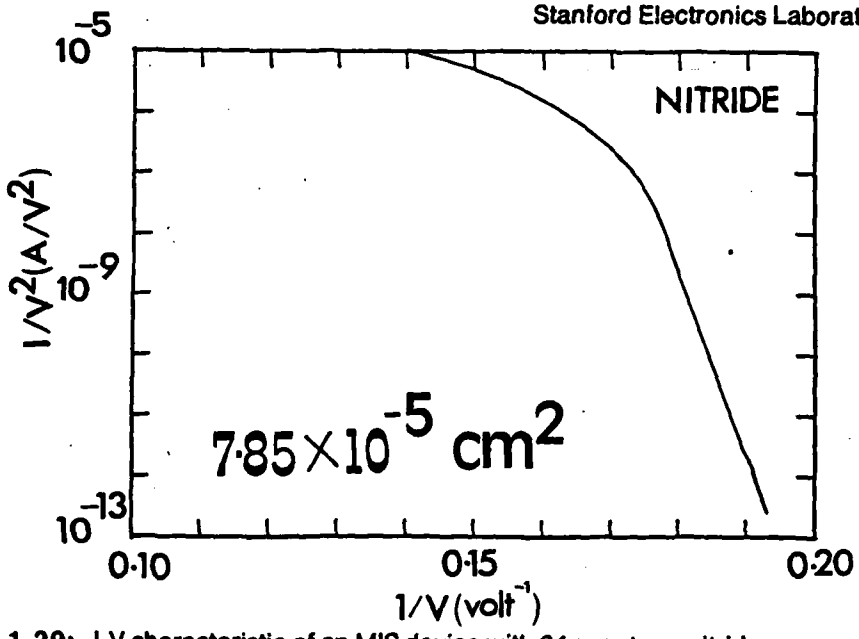


Figure 1-29: I-V characteristic of an MIS device with 64 angstrom nitride

of oxide thickness. However, this is not true for thermal nitrides in the ultrathin regime when direct tunneling through the nitride becomes important. Figure 1-30 shows the I-V characteristics of Al-gate devices (e-beam deposited) with gate areas of 7.85×10^{-5}, 3.14×10^{-4}, and 1.26×10^{-3} cm^2. The gate nitride was grown at 1100 °C for 2 hours resulting in about 40 angstroms of thermal nitride. By comparing this figure with that for 64 angstrom nitrides, we observe a sharp increase in conductivity through the nitride by going from 64 angstroms to 40 angstroms. The increase in conductivity is too high to be just attributed to the effect of a reduction in thickness of the nitride on F-N tunneling. In fact for nitride films of 40 angstroms or thinner the effect of direct tunneling on conductivity becomes a dominant factor. The excess amorphous silicon content of thinner nitride films might be an additional factor helping to increase the conductivity. The current densities in devices with three different areas are the same which is an indication of no edge effects on conductivity even in devices with gate nitride as thin as 40 angstroms. The effect of direct tunneling in thermal nitride films thinner than 40 angstroms implies that nitride films thinner than 40 angstroms may result in high gate leakage currents in IGFETs and low retention in EEPROMs. This was also verified by testing the devices with nitride insulator thicknesses ranging from 40 angstroms down to 20 angstroms.

Figure 1-31 shows the conduction characteristics of devices with nitroxide and SiO_2 gate insulators of gate electrode area 5.03×10^{-3} cm^2. 100 angstroms SiO_2 was grown in dry O_2 at 900 °C and then nitrided at 1000 °C for 4 hours. It can be observed that as a result of thermal nitridation there is an increase in conductivity through the device. Assuming that the current is mainly due to injection of electrons from the gate electrode (device in accumulation region), the nitridation-enhanced conductivity can be attributed to lowering of the barrier height at the surface due to the exchange of oxygen with nitrogen resulting in an enhanced tunneling probability.

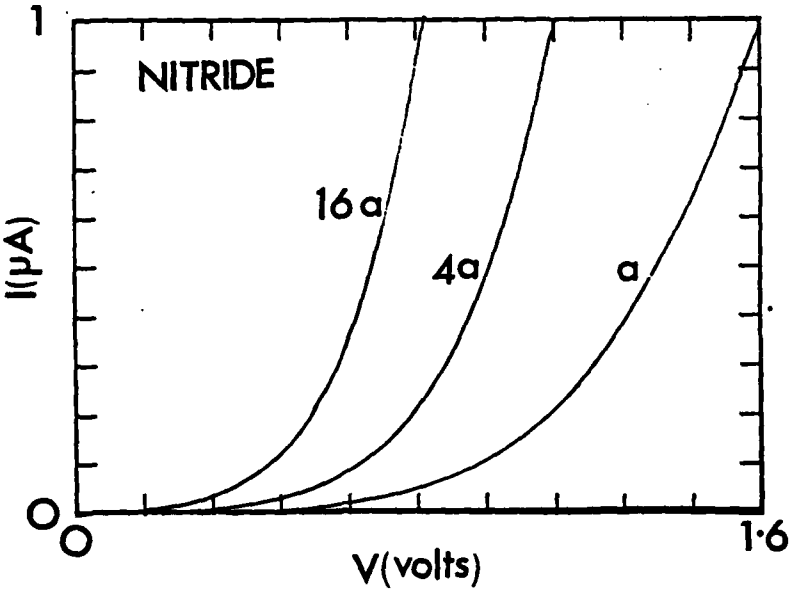


Figure 1-30: I-V characteristics of devices with 40 angstrom nitride

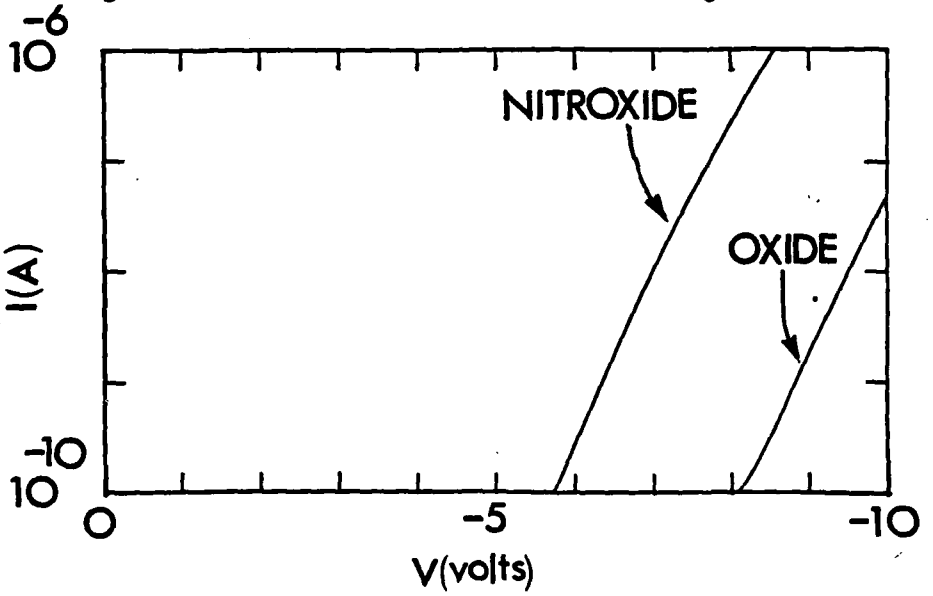


Figure 1-31: Conduction characteristics of devices with 100 angstrom oxide and nitroxide

Figure 1-32(a) illustrates a high frequency C-V plot of an MOS device with 100 angstroms SiO_2 before and after current injection of 1 μA for 15 seconds through the insulator (device in accumulation). The C-V curve was shifted to the right by about 0.5 volt which is an indication of electron trapping. Figure 1-32(b) shows the high frequency C-V characteristic of a device with about 60 angstroms thermal nitride. The C-V curve exhibited no hysteresis or shift during measurement and also after comparable charge injection indicating extremely low carrier trapping.

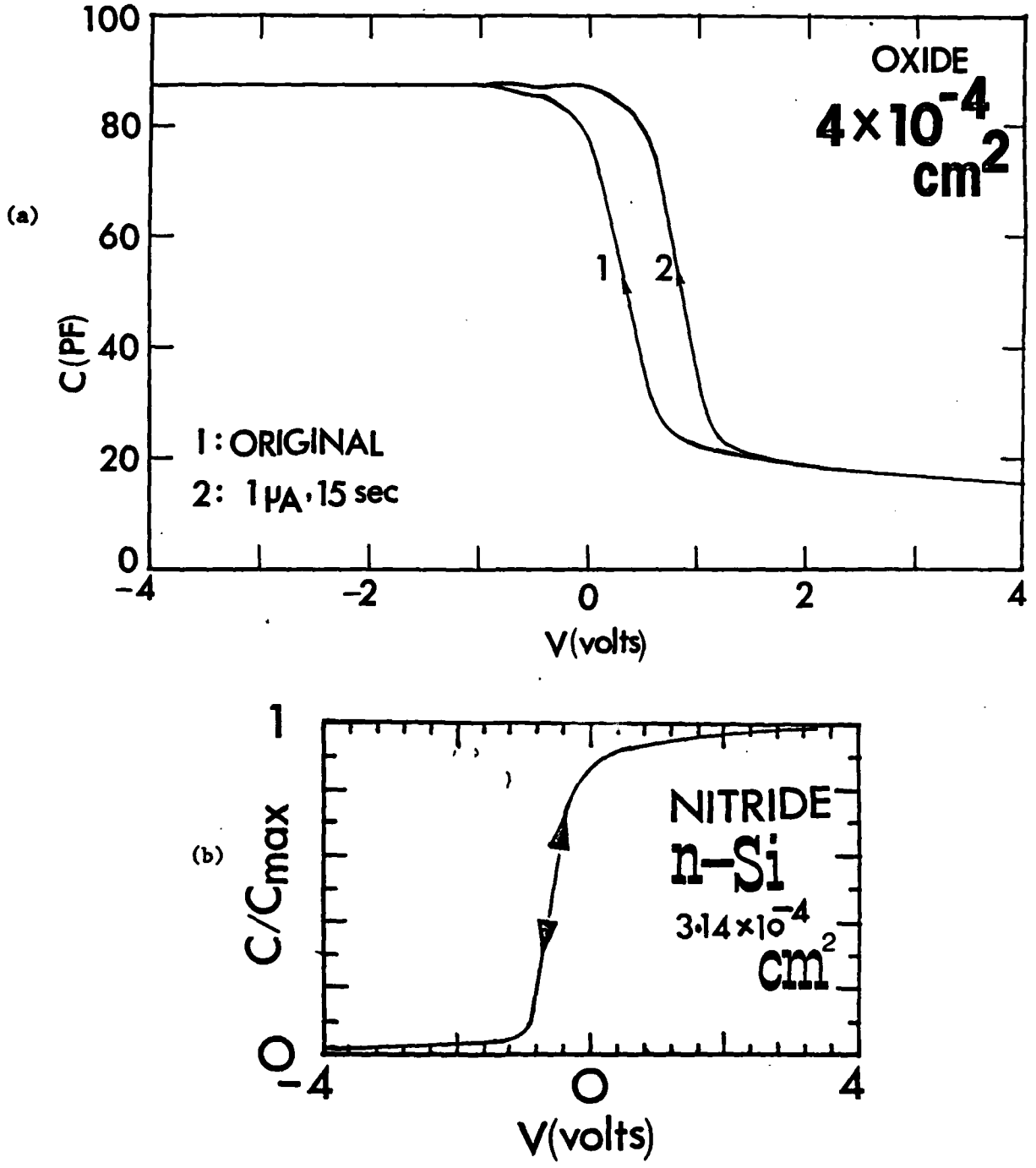


Figure 1-32: High frequency C-V for MIS devices with (a) 100 angstrom oxide and (b) 60 angstrom thermal nitride

Thermal nitride films show far superior electrical breakdown characteristics compared to oxide and

even nitroxide. Figure 1-33 shows the breakdown characteristic of devices with nitride gate insulators on n-type silicon. No destructive breakdown could be observed for currents up to a few hundred μA. The breakdown measurements on a device were reproducible indicating the nondestructive nature of breakdown for even very high current densities. This will be more clear when the time dependent electrical breakdown results are explained. Under the same conditions devices with 100 angstroms oxide and nitroxide showed destructive breakdown for much lower current densities. Nitroxide films were observed to withstand higher current densities than oxides before destructive breakdown. The breakdown field for thermal nitrides varies from about 10 MV/cm up to about 20 MV/cm depending on the electrode material, device area, and nitridation conditions.

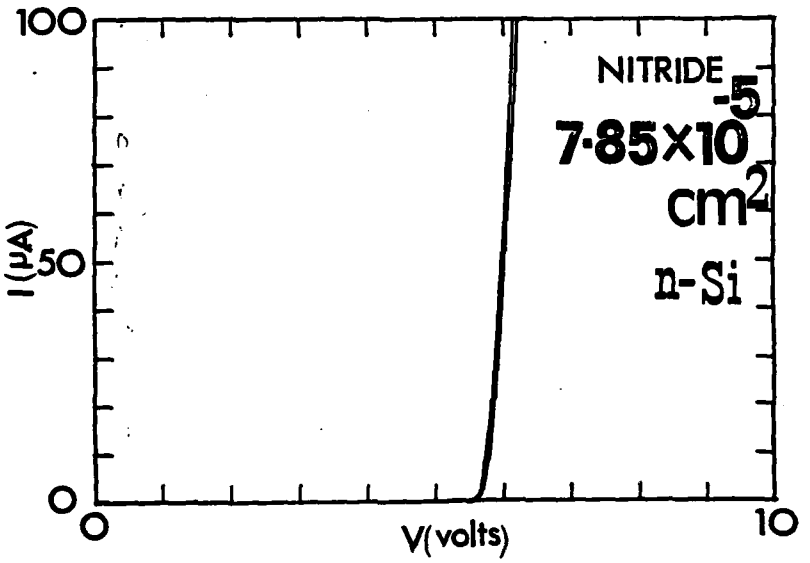


Figure 1-33: Breakdown characteristics of devices with thermal nitride insulators

Conduction characteristics can be influenced by trapping. The F-N plots in Figure 1-34 illustrate the effect of trapping on conduction in devices with 60 angstroms thermal nitride. I-V measurements were taken before and after injecting 25 μA into the gate for 100, 200, and 500 seconds. The rightmost curve shows the original conduction characteristic. Upon charge injection the I-V curves were originally shifted slightly to the left and then again back to the right. The shifts are very small and no destructive breakdown was observed even after 500 seconds current injection corresponding to about 160 C/cm^2 at a current density of 0.32 A/cm^2. This is much larger than the breakdown charge density in 100 angstrom thermal oxides at comparable current densities which was observed to be about 20 C/cm^2.

Time dependent electrical breakdown characteristics of devices with thermal nitride gate insulators were also examined. Figures 1-35(a) and 1-35(b) show these characteristics for devices with nitride

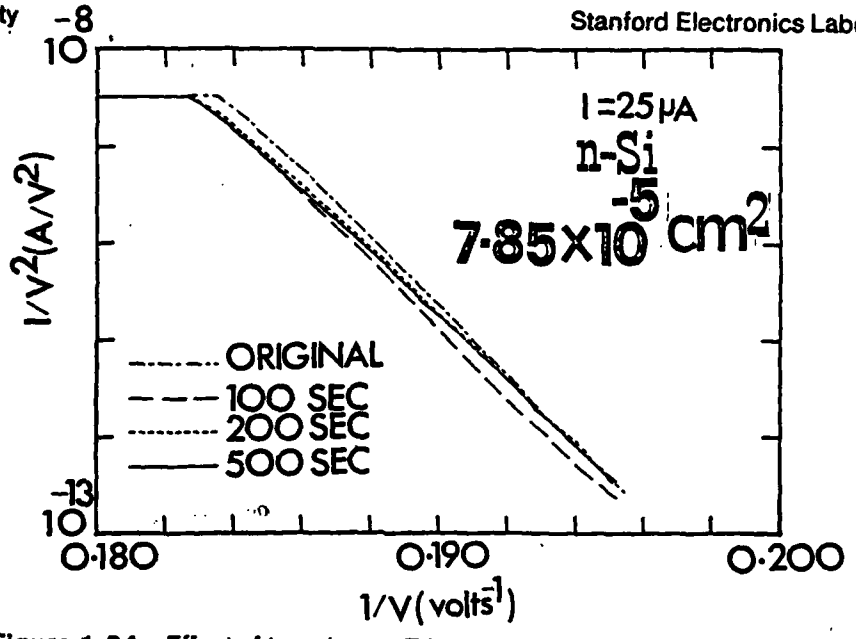


Figure 1-34: Effect of trapping on F-N conduction characteristics

gate gate insulators grown at 1230 °C for 1 hour and 4 hours on p-type and n-type silicon. For an injected current density of 1.27 C/cm^2, the devices with nitride grown for 1 hour on p-type silicon showed destructive breakdown after 400 seconds corresponding to about 510 C/cm^2 whereas the devices with nitride grown for 4 hours did not show any destructive breakdown even after 1000 seconds or injection of 1270 C/cm^2. These charge densities are much higher than that for 100 angstrom thermal oxides at comparable stress current densities which is less than 20 C/cm^2. In both figures the insets show the expanded voltage scale plots indicating hole trapping in the first case and electron trapping in the second one. The rate of trapping is extremely low which can be attributed to the high quality of the thermal nitride gate insulators and importance of field emission tunneling detrapping mechanisms in ultrathin gate insulators.

The interface quality and roughness has a direct relationship with the surface mobility of carriers in MISFETs. The interface roughness observed for thermal nitride is as good as those observed previously [5] for Si/SiO_2 structures. We measured a thickness of 41 angstroms for this film using an ellipsometer with the index of refraction fixed at 2.0. Using the cross-sectional TEM image of the same film and the (111) interplanar spacing as the measurement unit, the thickness is measured to be 43 ∓ 1.6 angstroms which is in good agreement with the ellipsometry result.

1.2.2.3 Summary

In summary, we have studied the electrical characteristics and interface morphology of thermal silicon nitride films. The results indicate extremely low trapping in these films. Films thicker than 40 angstroms can be used as gate insulators of field effect transistors; however, those thinner than that

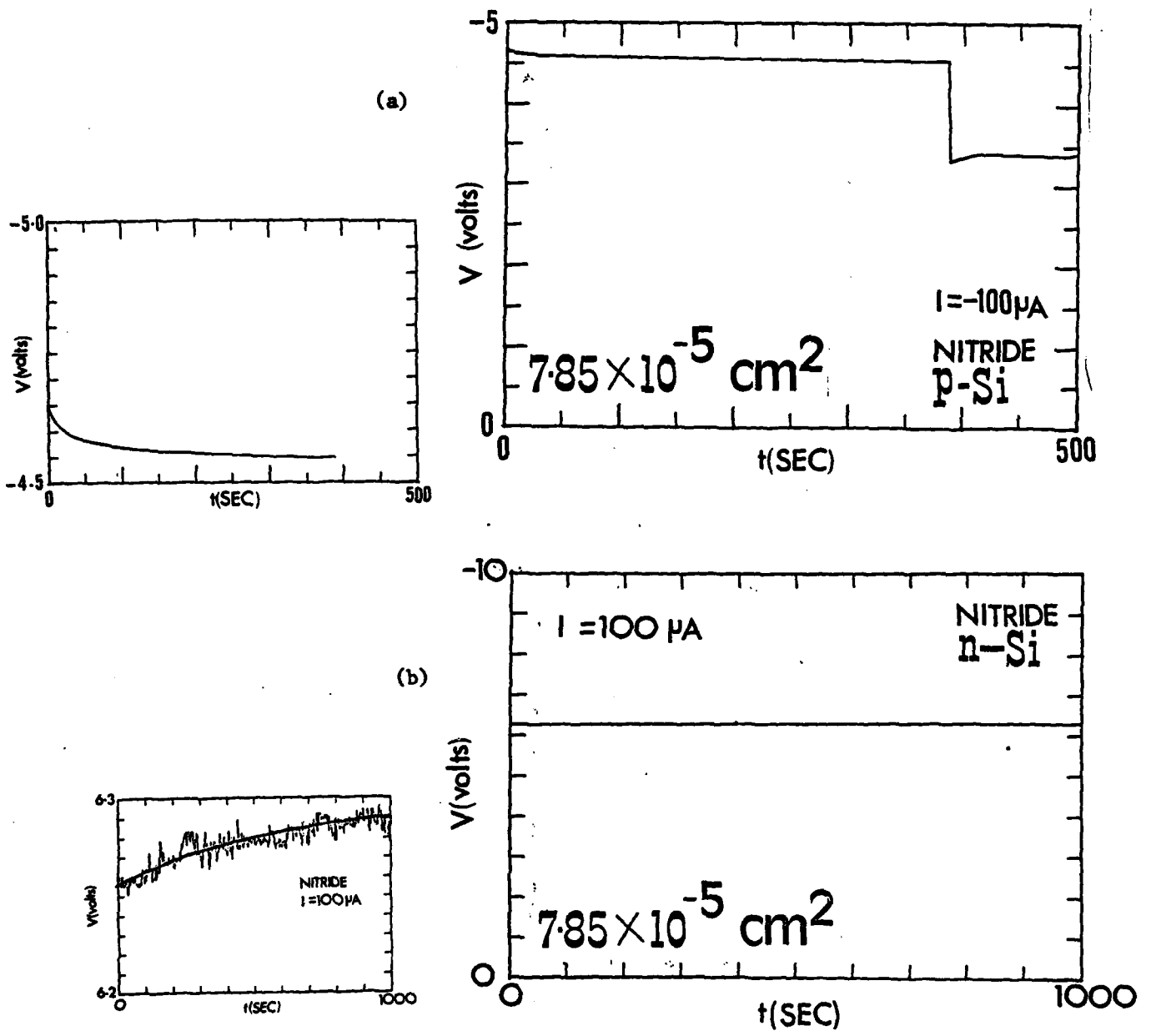


Figure 1-35: Time dependent electrical breakdown characteristics for devices with nitride grown at 1230 °C for (a) 1 hour on p-type and (b) 4 hours *on n-type Si*

show high leakage due to the quantum mechanical direct tunneling limitation. The interface abruptness and quality is comparable to high quality dry SiO_2. High density EEPROM and DRAM circuits as well as scaled VLSI IGFETs should find thermal silicon nitrides very useful tunneling and gate insulators.

1.2.2.4 References

1. Aucoin, R., Kirk, C., Naiman, M., and Terry, F. Kinetics of nitridation of silica films. Electrochem. Soc. 160th Meeting, 1981.

2. Chang, S., Johnson, N., and Lyon, S. "Capture and tunnel emission of electrons by deep levels in ultrathin nitrided oxides on silicon." *Appl. Phys. Lett. 44*, 3 (1984), 316.

3. Habraken, F., Kuiper, A., Tamminga, Y., and Theeten, J. "Thermal nitridation of silicon dioxide films." *J. Appl. Phys. 53(10)* (1982), 6996.

4. Hayafuji,Y., and Kajiwara,K. "Nitridation of Silicon and Oxidized-Silicon." *Journal of the Electrochemical Society* (Sept 1982), 2102.

5. Herman, F. Electronic structure of the Si-SiO_2 interface. Proc. of the Second International Conf., Insulating films on Semiconductors, Berlin, Germany, 1981, pp. 2.

6. Hirayama, M., Matsukawa, T., Arima, H., Ohno, Y., Tsubouchi, N., and Nakata, H. "Plasma anodic nitridation of silicon in N_2-H_2 system." *J. Electrochem. Soc. 131*, 3 (1984), 663.

7. Ito,T., Nozaki,T., Arakawa,H., and Shinoda,M. "Thermally Grown Silicon Nitride Films for High-Performance MNS Devices." *Applied Physics Letters 32(5)* (1978), 330.

8. Ito,T., Nozaki,T., Ishikawa,H., and Fukukawa,Y. Thermal Nitride Gate FET Technology for VLSI Devices. ISSCC Digest of Technical Papers, IEEE, 1980, pp. 74.

9. Ito, T., Arakawa, H., Nozaki, T., and Ishikawa, H. "Retardation of destructive breakdown of SiO_2 films annealed in ammonia gas." *J. Electrochem. Soc. 127*, 10 (1980), 2248.

10. Ito, T., Kato, I., Nakamura, T., and Ishikawa, H. Thermal nitride thin films for VLSI circuits. Electrochem. Soc. 163rd Meeting, 1983.

11. Ito, T., Nozaki, T., and Ishikawa, H. "Direct thermal nitridation of silicon dioxide films in anhydrous ammonia gas." *J. Electrochem. Soc. 127(9)* (1980), 2053.

12. Lai, S., Dong, D., and Hartstein, A. "Effects of ammonia anneal on electron trapping in silicon dioxide." *J. Electrochem. Soc. 129*, 9 (1982), 2042.

13. Moslehi,M.M. and Saraswat,K.C. Electrical Characteristics of Devices Fabricated with Ultrathin Thermally Grown Silicon Nitride and Nitroxide Gate Insulators. Proceedings, IEEE VLSI Symposium, IEEE, Maui, Hawaii, September, 1983.

14. Moslehi, M. M., and Saraswat, K. C. Thermal nitridation of silicon and silicon dioxide in a cold-wall rf-heated reactor. Proc of the Symp. on Silicon Nitride Thin Insulating Films, 1983, pp. 324-345. Electrochem. Soc. 162th Meeting

15. Terry, F., Aucoin, R., Naiman, M., Wyatt, P., and Senturia, S. "Radiation effects in nitrided oxides." *Elect. Dev. Lett. EDL-4*, 6 (1983), 191.

16. Wong, S., Oldham, W. and Grinolds, H. Anodic Si_3N_4 grown in a new plasma reactor. Third VLSI Symp., Dig. Tech. Papers, 1983.

17. Wong, S., Sodini, C., Ekstedt, T., Grinolds, H., Jackson, K., and Kwan, S. "Low pressure nitrided-oxide as a thin gate dielectric for MOSFETs," *J. Electrochem Soc. 130*, 5 (1983), 1139.

1.2.2.5 Recent JSEP Publications

1. Moslehi,M.M. and Saraswat,K.C. Electrical Characteristics of Devices Fabricated with Ultrathin Thermally Grown Silicon Nitride and Nitroxide Gate Insulators. Proceedings, IEEE VLSI Symposium, IEEE, Maui, Hawaii, September, 1983.

2. Moslehi, M. M., and Saraswat, K. C. Thermal nitridation of silicon and silicon dioxide in a cold-wall rf-heated reactor. Proc. of the Symp. on Silicon Nitride Thin Insulating Films, 1983, pp. 324-345. Electrochem. Soc. 162th Meeting

3. Moslehi, M. M., Saraswat, K. C., and Brauman, J. Electrical Characteristics and Interface Morphology of Ultrathin Thermally Grown Silicon Nitride Insulators. submitted to IEEE Trans. Elec. Dev.

1.2.3 Electronic Properties of Polycrystalline Silicon

Investigators: D.B. Kao and K.C. Saraswat

1.2.3.1 Scientific Objective

The major objective of this study is to investigate the oxide fixed charge, Q_F, and the interface traps, N_{it}, in polysilicon gate MOS devices and specifically to study the density of Q_F and N_{it} as a function of high temperature treatments in various ambients and the effect of device dimension scaling.

This work is important because most MOS devices today have Poly-Si gates, while most of the work on Q_F annealing has been based on data from aluminum gate devices where the bare gate oxide is quite sensitive to processing conditions before the final low temperature metalization step. The Q_F triangle, as shown by Deal,et al. [2] illustrates that these charges vary with processing temperature and ambient. In an earlier experiment [3], we reported that large area Poly-Si gate capacitors are insensitive to processing conditions, because polysilicon shields the gate oxide from O_2 in the ambient. That finding led us to pursue the edge effects of scaled down Poly-Si gates, especially the peripheral Q_F generated by the diffusion of oxygen at the edges of the gate. This peripheral Q_F will be important for total Q_F control in small devices.

Our results indicate that, even for gate width as small as 1.25 μm, Q_F underneath the polysilicon gate is unaffected by further processing steps, including high temperature oxidizing ambients. A two-dimensional oxygen diffusion model is proposed to explain this phenomenon.

1.2.3.2 Progress

Experimental

Polysilicon gate MOS capacitors with finger structures were fabricated using a dual oxide approach with a gate oxide of 630 angstroms, and thick field oxide of 7400 angstroms. All capacitors have the same area. The width of the fingers and the spacing between the fingers were kept equal and varied from 10 μm to 1.25 μm resulting in a larger perimeter for smaller finger widths. The wafers were annealed in O_2 and *Ar* at different high temperatures and for different lengths of time. After each high temperature anneal, the wafers were annealed in forming gas at 450°C for 30 minutes, before C-V measurements were taken to determine V_{FB} and Q_F. From the difference between high-frequency and quasi-static data, D_{it} was determined to be less than $2\text{x}10^{10}$ cm^{-2}. The low D_{it} value indicates that hydrogen in the forming gas diffuses through polysilicon grain boundaries and anneals the interface traps sufficiently. Figure 1-36 shows a series of high frequency C-V curves for devices with different perimeter to area ratios. The fringing capacitance is evident when the devices are in inversion, resulting in the different values for C_{min}. It is negligible in accumulation. This is understandable because in accumulation, the oxide capacitance dominates and the fringing capacitance is negligible because of the thin gate oxide. When the device is in inversion, however, silicon depletion capacitance dominates. In this case, the fringing field extends the depletion region outside the gate and reduces the maximum depeletion width, thus increasing the silicon depletion capacitance and the total capacitance. The inversion region fringing capacitance is proportional to the perimeter to area ratio.

Results and Discussion

Experimental results of annealing are shown in Figure 1-37. The normalized $V_{FB}(V_{FB}/V_{FB(initial)})$ is plotted for a sequence of successive annealing conditions. It can be seen that the capacitors do not show any significant changes in V_{FB} or Q_F after anneal in O_2 at 900°C and 1000°C for different periods of time and different O_2 partial pressures, or after a final Ar anneal at 1000°C. This is true for devices of all dimensions, including the ones with 1.25 μm wide fingers. This result indicates that there is negligible change of Q_F in the gate oxide underneath the polysilicon gate. Since Q_F is a product of the oxidation process, a plausible explanation is that there is simply very little oxygen underneath the polysilicon gate, which may be as narrow as 1.25 μm. This seems to be in obvious contradiction to what would be predicated by the high diffusivity of O_2 in SiO_2, about 10^{-8} cm^2/sec. To resolve this dilemma, a study of the diffusion of O_2 in the gate oxide underneath polysilicon was undertaken.

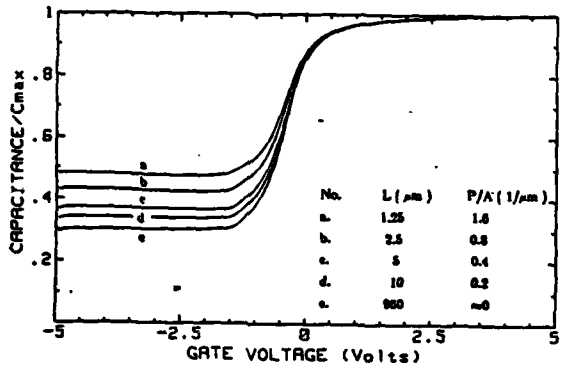
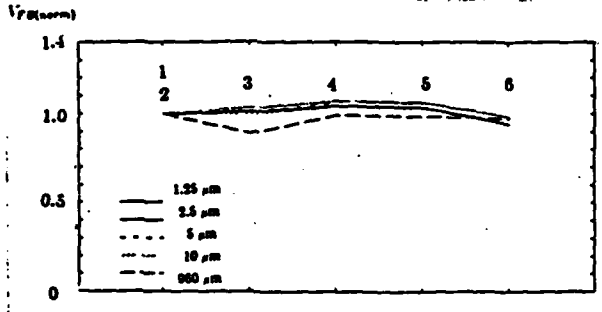


Figure 1-36: High-frequence C-V plots for different finger widths (L), or perimeter to area ratiois (P/A). The inversion region capacitance is proportional to P/A.



Annealing Sequence:

1.	1000° C	Ar	30 min
2.	900° C	Diluted O_2	30 min
3.	900° C	O_2	30 min
4.	1000° C	O_2	15 min
5.	1000° C	O_2	30 min
6.	1000° C	Ar	30 min

Figure 1-37: Normalized flat band voltages, $i\langle V_{FB(norm)}\rangle$, defined as $i\langle V_{FB}/V_{FB(initial)}\rangle$ for a series of annealing conditions. There is negligible change in V_{FB} caused by peripheral Q_F under Poly-Si gates.

The Deal-Grove oxidation model [2] can be extended to two dimensions [1]. Our case is a two-dimensional steady-state diffusion problem with a source and different sinks:

$$D\nabla^2 C = \frac{\partial C}{\partial t} = 0 \quad Laplace's\ Eq.$$

$$D\frac{\partial C}{\partial y} = h(C^* - C) \quad at\ O_2\ source$$

$$D\frac{\partial C}{\partial y} = k_s C \quad at\ Si/SiO_2\ interface$$

$$D\frac{\partial C}{\partial y} = 0 \quad at\ non-oxidizing\ interface$$

Numerical solution was carried out with an iterative finite-difference boundary value method. Figure 1-38 shows the simulated contour plots of O_2 concentration near the edge of a nitride cap (non-oxidizing boundary) and of a polysilicon gate (oxidizing boundary), respectively. Figure 1-39 shows the O_2 concentrations at the SiO_2/Si-substrate interface, for both the nitride case and polysilicon case. It can be seen that even underneath nitride, the steady state O_2 concentration under the cap is relatively small, despite the high diffusivity of O_2, consistent with result shown in [1]. This makes sense because the oxidizing boundary of the *Si* surface serves as a sink for O_2, limiting its distribution deep underneath the gate. The fast-oxidizing polysilicon consumes even more O_2, thus pulling most O_2 away from the SiO_2/Si-substrate interface, leaving even less O_2 available for Q_F generation in the interface.

1.2.3.3 Summary

In conclusion, our study shows that the polysilicon gate not only acts as an oxygen barrier above the gate oxide, it also keeps oxygen away from the SiO_2/Si-substrate interface under the gate edges. Even for very small polysilicon gate dimensions, Q_F anneals under the gate independent of previous process history. In addition, subsequent high temperature exposures to oxidizing ambients have no effect on Q_F. However, as devices are scaled down further, other edge effects may become important: such as fringing fields, and non-uniform gate oxide due to polysilicon oxidation.

1.2.3.4 References

1. Chin,D. J., Oh,S. Y., Hu,S. M., Dutton,R. W., and Moll,J. L. "Two-Dimension Oxidation Modeling." *IEEE Trans. on Electron Devices ED-30* (July 1983).

2. Deal,B.E. and Grove,A.S. "General Relationship for the Thermal Oxidation of Silicon." *J. Appl. Phys.* (December 1965).

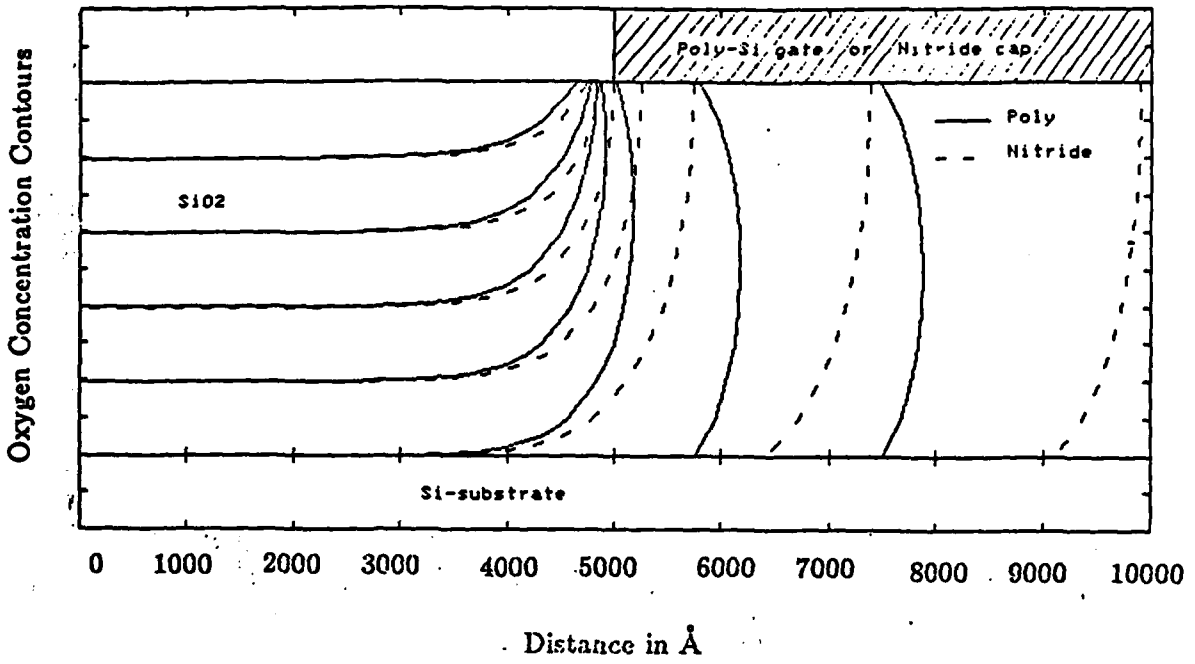


Figure 1-38: Simulated O_2 concentration contours in SiO_2 near the edge of a Poly-Si gate (solid lines), and a Nitride cap (dotted lines). Poly-Si gate, being an oxidizing boundary, consumes O_2 and pulls O_2 away from the SiO_2/substrate interface.

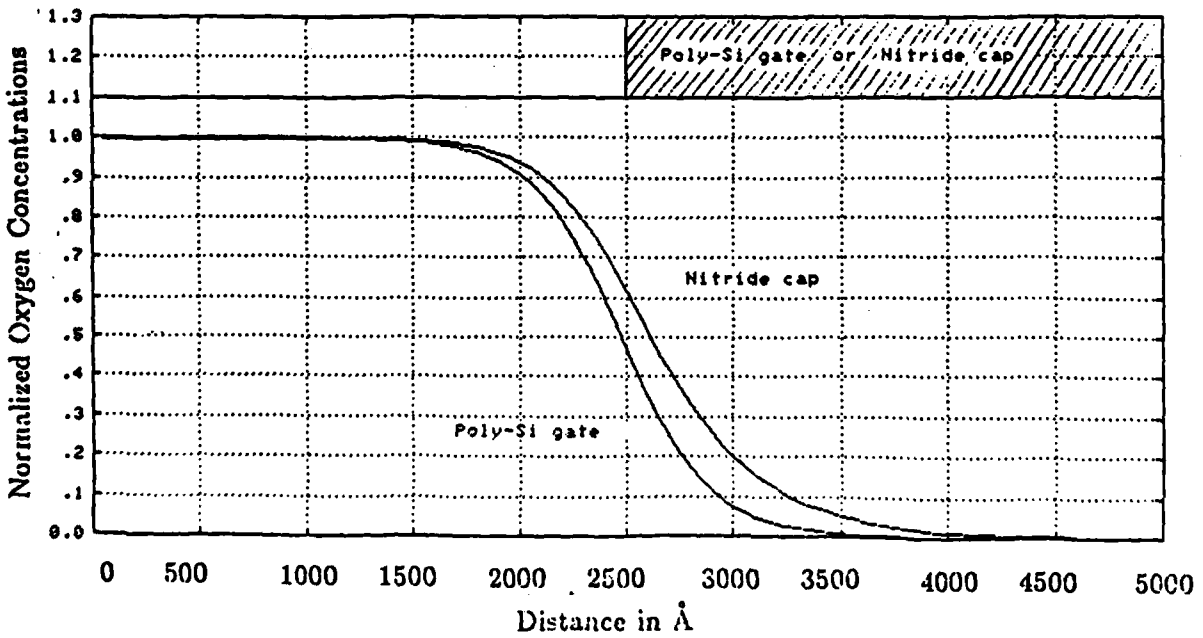


Figure 1-39: Simulated O_2 concentration along the SiO_2/substrate interface. The O_2 concentration under Poly-Si gate (solid curve) is lower than that under the Nitride cap (dotted curve), because polysilicon gate oxidizes and consumes O_2.

3. McVittie,J. P., Chang,G., Kao,D. B., and Patton,G. L. Annealing of Fixed Charges in Poly-Si Gate MOS. ECS Meeting Extended Abstract, May, 1983.

1.2.3.5 Recent JSEP Publications

1. Kao,D.B., Saraswat,K.C., and McVittie,J.P. Annealing of Oxide Fixed Charges in Scaled Polysilicon Gate MOS Structures. IEEE Semiconductor Interface Specialist Conference, December, 1983.

2. Kao,D.B., Saraswat,K.C., and McVittie,J.P. Annealing of Oxide Fixed Charges in Scaled Polysilicon Gate MOS Structures. submitted to IEEE Transactions on Electron Devices

3. McVittie,J. P., Chang,G., Kao,D. B., and Patton,G. L. Annealing of Fixed Charges in Poly-Si Gate MOS. ECS Meeting Extended Abstract, May, 1983.

1.2.4 Ohmic Semiconductor Contacts with Low Minority-Carrier Recombination Velocity

Investigator: R. M. Swanson

1.2.4.1 Scientific Objectives

This research program has aimed at developing SIPOS (Semi-Insulating Poly Silicon) emitters for bipolar transistor applications.

1.2.4.2 Progress

Using technology improvements discussed in previous reports the emitter Gummel number was increased two orders of magnitude over that attainable with a conventional diffused emitter. Due to this success, alternative support has now been obtained to begin looking at the impact these emitters might have the performance of high speed bipolar devices. A considerable speed increase is expected through the use of SIPOS emitters.

The relaxation of design constraints that result from the reduction of J_{oe} through SIPOS emitters provides greater flexibility and may suggest new guidelines for device optimization. It has been demonstrated that shallow homojunctions made in silicon are limited by materials parameters associated with high level doping effects to values in excess of $1x10^{-12}$ A/cm^2. Examination of parameters on a phenomenlogical level indicate that several alternate structures can reduce J_{oe} several orders of magnitude below this "fundamental" limit; however, the SIS structure incorporating a thin interfacial silicon dioxide that both passivates the interface and imposes a transport barrier to holes appears to offer a solution that is compatable with standard process technology. Modeling of both static and dynamic behavior of this structure produced guidelines regarding the extent of outdiffusion that could be tolerated. It was seen that reduction of J_{oe} involved attaining a profile with

sufficiently high surface concentration to achieve a low equilibrium surface hole density, yet shallow enough to minimize the impact of Auger recombination. High frequency performance which relies on the minimization of hole storage, was shown to favor the shallow structures as well. Reduction of the extent of the outdiffused layer consistent with the surface concentration requirement was shown to favor both static and dynamic performance.

Experimental BJT's incorporating Poly and SIPOS contacts were used to develop the fabrication technology for achieving low static values of J_{oe}. It was shown that for POLY emitters, that the presence of the interfacial oxide is mandatory for good performance. "Intimate" POLY contacts behaving essentially as extensions of the monocrystalline regions, do not seem to be able to offer much in the way of achieving low absolute values of J_{oe} although relative enhancements are readily attained. Although no attempt was made to understand hole transport mechanisms in heavily doped POLY, it is felt that they are understood albeit on an unsophisticated phenomenlogical level. The situation for SIPOS contacts is different. Low oxygen content films behaved surprisingly well. Although all indications point to an interfacial barrier action for this type of contact as well, the exact nature and even origin of this interfacial layer is poorly understood. In part, this is attributable to a lack of adequate control over the SIPOS deposition ambient.

1.2.4.3 Future Plans

Further investigation may serve to clarify some of these issues. Since the most interesting physics appears to lie in the low oxygen content SIPOS films, tighter control over residuals in the deposition ambient is necessary. A more sophisticated wafer loading system is needed to limit the growth of unintentional exides, and special care must also be taken to avoid contamination by residual organics. If the interfacial oxide is found to result from the annealing of the SIPOS film itself, then the kinetics of this reaction need to be studied. The long term stability of these interfacial layers has not been established; work on possible failure mechanisms is needed. Characterization of majority carrier series resistance was only cursorily done, and only for the SIPOS contacts. This is a major drawback, as it makes evaluation of the relative merits of SIPOS and POLY contact structures difficult. This is certainly an area that needs extensive characterization before application of these structures to high speed or high current density applications can be considered practical.

The dynamic performance of these contact structures was not experimentally investigated. Actual device geometries optimized to take advantage of the low J_{oe} need to be fabricated to see if the potential gains that were suggested can be realized in practice. For application to the point contact solar cell, the performance of the P-type counterpart must be established. Comparison to the N-type may also shed some light on the physics of these contacts.

1.2.4.4 Recent JSEP Publications

1. Kwark,Y. and Swanson,R.M. "Optical Absorption of Thin SIPOS Films." *J. Electrochemical Soc.* 129, 1 (January 1982), 197-201.

2. Yablanovich, E., Swanson, R. M., and Kwark, Y. H. An n-SIPOS:p-SIPOS Homojunctionn and a SIPOS-Si-SIPOS double heterostructure. Proceedings 17th IEEE Photovoltaics Specialists Conference, 1984.

1.2.5 Interaction of Transition Metals with Silicon Surfaces

investigator: W. E. Spicer, I. Lindau

1.2.5.1 Scientific Objective

During this reporting period we have completed the first preliminary investigation of the interaction of transition metals with Si surfaces. The primary objective was to study interaction on well-characterized, i.e. atomically clean and structurally ordered, Si surfaces. To this end the interfaces were prepared by cleavage of Si *in situ* with subsequent metal deposition under ultrahigh vacuum conditions.

1.2.5.2 Progress

Mo was deposited onto the in situ cleaved Si(111) 2 x 1 surface with coverages ranges from 0.1 to 20 atomic layers [1]. The induced changes in the electronic structure was studied by photoemission using synchrotron radiation in the soft x-ray region. This technique was also used to determine the abruptness of the interface. Interestingly, the room temperature results showed that the interface is abrupt on an atomic scale, contrary to results we have obtained earlier for Pd/Si and Pt/Si where intermixing takes place over several layers. In the latter two cases a small amount of oxygen (i.e. about one monolayer) will drastically reduce the interdiffusion. In the case of Mo the effect of oxygen is much less pronounced [2]. The next step in this work will be to examine the Schottky barrier heights in these different situations. As far as the chemical reactions are concerned we observe silicide formation already at room temperature at the low coverages. (The Mo bulk silicide forms at 525°C. Even for submonolayer coverages the Mo-Si bonding has the same electronic characteristics as the bulk silicide, Mo-Si_2. Thus on an atomically local level there is a trend to have the bulk Mo-Si configuration.

1.2.5.3 References

1. Rossi, G., Abbati, I., Braicovich, L., Lindau, I., Spicer, W. E., del Pennino, U., Nannerone, S. "Exploiting Photon Energy Dependence in Photoemission from Si(111)-Mo Interface." *Physica B 795* (1983), 117-118.

2. Rossi, G., Abbati, I., Lindau, I., Nogami, J., Spicer, W. E. The Electronic Structure of Clean and Oxygen Exposed Si(111)-Mo Interfaces. In preparation for submission to Phys. Rev. B.

1.2.5.4 Recent JSEP Publications

1. Rossi, G. and Lindau, I. "Compound Formation and Bonding Configuration at the Si/Cu Interface." *Phys. Rev. B 28* (1983), 3597.

1.2.6 Interaction of Impurities with Silicon Surfaces and Interfaces

Investigator: C. R. Helms

1.2.6.1 Scientific Objective

In past periods of this contract, the objective of this part of the program was to determine the effect of arsenic, boron, and other impurities on the electronic structure of the silicon free surface. The first phase of this study was completed last year with the Ph.D. Dissertation of S. C. Perino entitled "The Electronic Structure and Deposition Kinetics of Arsenic on the Silicon Surface" [2]. In this period we have continued our studies specifically to determine the effect of interfacial contamination layers on the Schottky barrier height of silicon-metal contacts.

1.2.6.2 Progress

In this period, we have invetigated the effect of the presence of thin (< 10 angstrom) interfacial layers of oxide and carbon on the Schottky barrier height for selected silicon metal contacts. These contamination layers can be deposited and indeed represent residues from some of the standard IC Chemical Cleaning procedures [1]. Of interest here was the effect of the thin oxide left on the surface after the "RCA" clean with the final HF etch left out and the effect of thin carbon residues left after the full RCA clean including the HF etch final step. We find that the "RCA oxide" residue has a large effect on Schottky barrier height whereas the carbon residue has very little effect. For example, the thin RCA oxide (10) can increase (decrease) the Schottky barrier of Ti on p(n) type silicon from $\propto$0.6 (0.5) eV to 0.9 (0.2) eV. Although this is desirable for some applications, this effect is not thermally stable for temperatures $\propto$200 °C and can lead to unreliable, unreproducible barrier values. The initial stages of this investigation are complete and follow on fundinng for further studies based o these results with the goal of establishing a complimentary MESFET technology has been obtained from the Semiconductor Research Corporation.

1.2.6.3 References

1. Meindl, J. D. et al. Annual Progress Report, 1 April 1982 - 31 March 1983. Tech. Rept. 2, Stanford Electronics Laboratories, Stanford University, 1983.

2. Perino,S.C. *The Electronic Structure and Deposition Kinetics of Arsenic on the Silicon Surface.* Ph.D. Th., Stanford University, Elec. Engr. Dept., 1982.

1.2.7 Interconnections for High Density, High Performance VLSI

Investigators: R. F. W. Pease, P. de la Houssaye, G. L. Yoffe

1.2.7.1 Scientific Objectives

One result of the increasing scale of integration is that the packing density and performance of VLSI circuits is at present limited by interconnects and not by intrinsic speed of the active devices. The aim of this project was to investigate ways in which the limits posed by interconnects might be overcome so that advances in the more fundamental properties of the semiconductor devices will once again lead to advances in terms of improved system performance.

Interconnects can limit the performance of VLSI circuits in a number of different ways. The large fraction of space occupied by interconnects leads to long transmission paths for signals. Thus in the most basic case, in which the interconnect acts as a lossless, dispersionless line, there will be a propagation delay set by the parameters of the line. At present I.C. metallization paths are far from acting as such lines and the delays are considerably longer than those of a line propogating signals at a speed c/2. With the advent of fine line lithography the number of squares of long metal runners has increased and the resistance of the line has become appreciable in that long lines act as distributed RC networks (each with a characterister time constant). Shorter lines still act a lumped capacitor that must be charged or discharged in active devices [1]. In circuits with large currents being drawn the problems of electromigration can be serious and voltage drops can also be significant.

Among the proposals for ameliorating the condition imposed by todays metallization are:

1. Improve the metallurgy to improve resistance to electromigration.
2. Operate at low temperature to improve electrical conductance.
3. Exploit the vertical dimension to improve the conductance per square and also reduce the area taken up by interconnect and hence reduce interconnect length.

1.2.7.2 Progress

The first approach was to investigate the possibilites of improved resistance to electromigration of aluminum alloy runners by selective annealing with a scanning electron beam. The principle in to induce all grain boundaries to be perpendicular to the direction of current flow. Previous work has shown that such a "bamboo" structure leads to greatly improved mean time to failure [3] but that the structure occured naturally only under restricted conditions.

The results obtained showed morphological evidence of some local bamboo structure but the practicality of achieving such a structure repeatedly over long lengths of metal over a variety of underlying films as occurs in an integrated circuit) seemed remote.

However the ability to use the heating effect of the beam to fashion the metal led to other interesting possibilities with much greater potential impact on the interconnect problem. One of the main difficulties of exploiting the vertical dimension to achieve many layers of interconnect is that of achieving a planar structure containing arbitary pattens of metal and insulator. In particular the problems of filling "posthole" vias with metal has proved particularly awkard. The possibility of using the directed energy of a laser or electron beam to bring about controlled local melting of the metal appears quite promising. We have investigated one suggested scheme depicted in Figure 1-40.

The experiments carried out so far have employed lines rather than individual holes. The oxide thickness is 0.5 μm and the metal, pure aluminum, was deposited by evaporation and patterned lift-off. Raster scanning with a 20 kV, 3 μm diameter, electron beams of 20 μA current resulted in local melting and planarization was accomplished in some instances (Figure 1-41). It may be that transient large area heating, such as can be obtained with a pulsed laser, amy be more suitable and that undue heating of underlying layers can still be avoided. Thus it appears that transient heat treatment which has been so successful in fashioning semiconductors may also have a big impact in solving some of the metallization problems. Any successful realization of this technology will require fundamental studies of the insulator surface and of the metal/insulator interface. Nonetheless, the technonlogical rather than scientific emphasis of this project as it is now configured is leadinng us to seek support from programs with more directed aims than JSEP.

1.2.7.3 References

1. Sinha, A. K., Cooper, J. A., Jr., and Levinstein, H. J. "Speed Limitations Due to Interconnect Time Constants in VLSI Integrated Circuits." *IEEE Elec. Dev. Lett. EDL-3* (April 1982), 90-92.

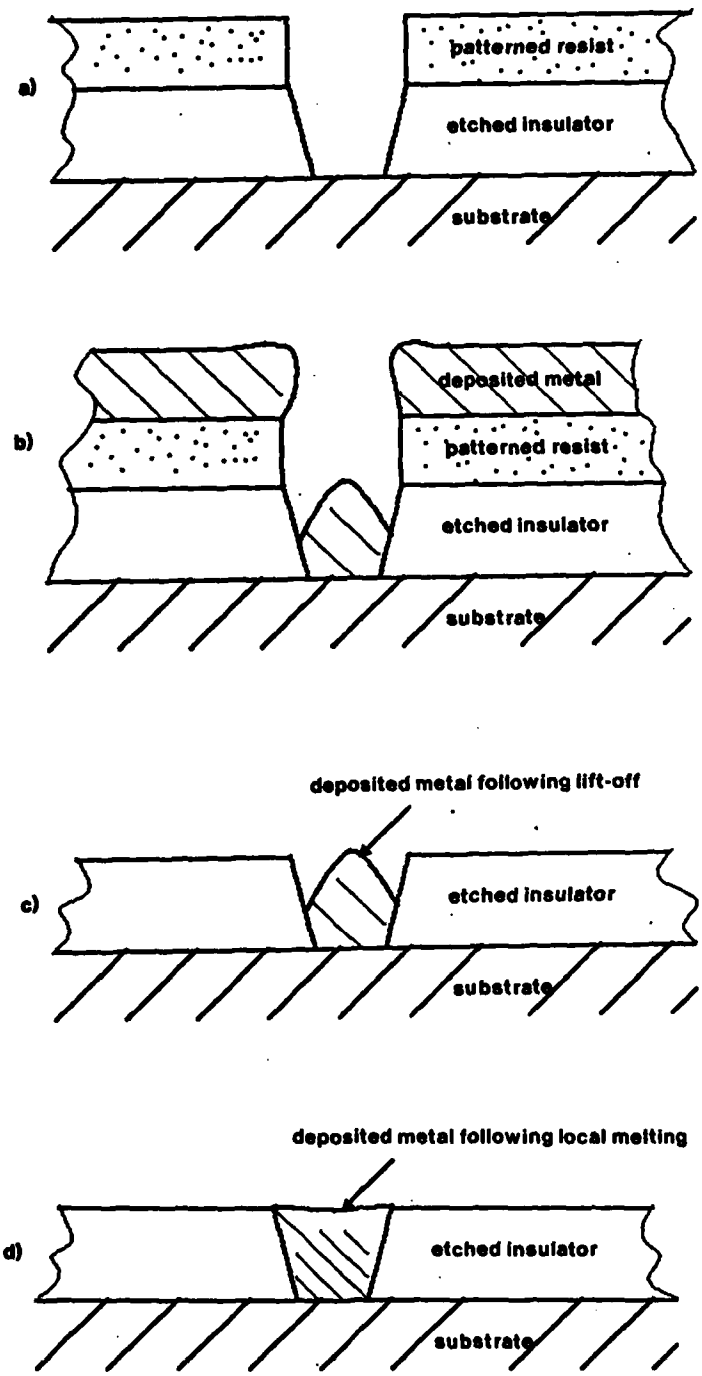


Figure 1-40: Steps in process leading to a planar structure containing arbitrary patterns of metal and insulator. The critical steps are depositing sufficient metal to fill etched features in the insulator and controllably melting the deposited metal to planarize the top surface without damaging underlying layers [2].

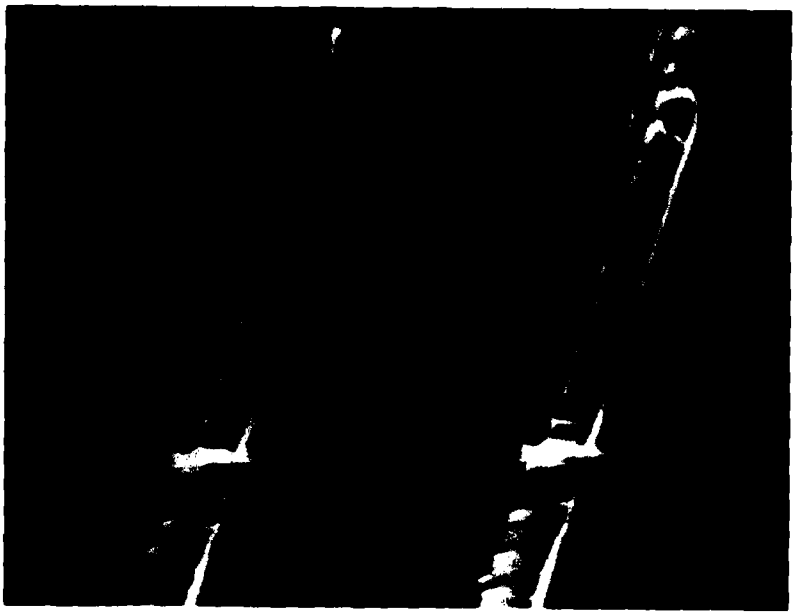


Figure 1-41: Scanning electron micrograph of aluminum lines in 1 μm-wide SiO_2 trenches locally melted (in lower 1/3 of picture) to form a nearly planar structure

2. Tuckerman, D. B. Unpublished Work.

3. Vaidya, S., Fraser, D. B. and Sinha, A. K. Electromigration Resistance of Fine-Line Al for VLSI Applications. Proceedings 18th IEEE Reliability Physics Symposium, April, 1980, pp. 165-170.

1.2.8 Study of Compound Semiconductor Device and Materials Physics

Investigator: James Harris

1.2.8.1 Scientific Objective

The objective of this project is to investigate heterojunction, quantum well and superlattice concepts and their application to new electronic devices. The long range objective is to study devices utilizing structures of ultra-small dimensions where quantum size effects totally dominate the transport properties and energy states within the structures. These new device concepts may provide the foundation for an electronics technology with vastly superior performance compared to devices based upon current device concepts.

1.2.8.2 Progress

Molecular Beam Epitaxy (MBE)can readily produce structures of the required dimensions (<200 Angstroms) and is thus a major facility required to carry out research in this area. Since this is a new project at Stanford, the first year objectives were to define a program in III-V compound semiconductor devices, acquire funding for an MBE system and begin to develop the necessary processing and characterization facilities to carry out research in this area.

One of the major accomplishments this year was the award of a DARPA program to fund purchase of an MBE system. A two chamber Varian MBE system will be delivered in Aug. 1984. This system will be available to carry out the research on ultra-small dimension structures proposed in this project.

Examination of various device concepts during the past year has led us to the conclusion that the next frontier in device concepts will not be an evolutionary one, but a revolutionary one. That is, even the new hetero-junction concepts, such as the MODFET and heterojunction bipolar transistor, are still largely based upon conventional device physics and carrier transport concepts. These structures will certainly be advanced in the coming years and provide increased speed, and performance for ICs. However, as device dimensions continue to shrink, quantum phenomena are going to become the dominant device factor. There are currently only vague ideas on the use of quantum wells for storage of electrons and resonant tunneling between wells as the dominant transport mechanisms between regions. It is time to begin to seriously investigate such concepts. We have defined a research program to investigate such concepts and to develop analytical techniques to provide the necessary characterization and feedback for understanding structures with 10-100 Angstrom dimensions. This program is outlined in detail in the proposal for the follow-on JSEP program.

In order to study quantum well structures, we must first understand the physics and control of the AlGaAs/GaAs interface, particularly, the asymmetries which are dependent on the growth sequence. To begin developing a process capability for III-V materials and to investigate the AlGaAs/GaAs interface, we selected a MODFET structure as a starting point. This structure is based upon the GaAs/AlGaAs interface, requires MBE growth capability and is very sensitive to growth and process induced changes in the interface.

A mask set was designed with the aim of being able to measure a whole host of parameters on the same die with MODFET structures. Chip layout is such that the left side of the die can be split off, bonded and cooled to liquid nitrogen or helium temperatures. Of primary importance on this side are the Hall bars, one of which is gated. Also included are fat gate and small geometry MODFETs. On the other half of the die are more MODFETs, a large pad for C-V or DLTS measurements, and an unused area for optical characterization, such as photoluminesence. Features exist on this side for determining various process parameters such as implant activation, contact resistance, quality of isolation etc. Two thirty-nine element ring oscillators, one for depletion and one for enhancement style MODFETs, each with their own output are also included.

With this mask set it should be possible to determine the mobility of the two-dimensional electron gas at the heterojunction interface as a function of both temperature and gate bias for a given sample. Both the thickness of the AlGaAs layer and type of surface passivation layer, if any, can also be varied from wafer to wafer.

From the gated Hall bar measurements and other measurements available on the die, we hope to determine the effect of filling different quantum levels at the interface. This investigation will include a study of the mobility of the carriers when the upper levels become filled and the scattering processes which are effective in the various regimes. A second effort is in progress to predict the two-dimensional electron gas mobility using scattering theory under various conditions of doping and temperature.

2. INFORMATION SYSTEMS

2.1 Real Time Statistical Signal Processing

Principal Investigator: T. Kailath

2.1.1 Scientific Objectives

The goals of this research program were to study emitter location problems and in particular focus on methods for determining the number of sources and processing array data when the signal is completely coherent with one or more interferences.

2.1.2 Progress

2.1.2.1 Determining the Number of Sources

A new approach to the problem of determining the number of sources for a passive array was developed [6]. The method is based on *information theoretic criteria* concepts for model selection introduced by Akaike (A Information Criteria - AIC) and Rissanen (Minimum Description Length - MDL) .The conventional approach for determining the number of sources in the eigenstructure framework were based on hypothesis testing that required definition of thresholds. The new approach does not require any *subjective* threshold settings. The number of sources is determined merely by minimizing the AIC or MDL criteria.

It was analytically proven that the MDL criteria yields consistent estimates for the number of sources whereas the AIC overestimates their number.

Simulation studies were carried out to verify these methods and yielded good results under varying situations including low signal to noise ratios, small number of data samples and closely spaced signals.

The new approach is equally applicable in other areas where eigenstructure methods have been used. Some examples are determining the number sinusoids in time series data, the number of poles from the natural response of a linear system and the number of overlapped echoes in backscatter data typical in radar, etc.

2.1.2.2 Coherent Signals and Interference

The key concept here has been the use of *spatial smoothing* to *decorrelate* coherent arrivals at the sensor array thus effectively solving the coherent signal and interference problem. It is of interest to note that the problem of dealing with fully coherent signals and interference has been outstanding for nearly two decades after it was found that optimum beamforming techniques do not work in these conditions.

In [5] we show how spatial smoothing can be used to *restore the rank* of the covariance matrix of the signals and coherent interference impinging on an array. This enables the use of eigenstructure methods to determine the directions of arrival of sources while still yielding estimates which are unbiased and asymptotically exact.

In [3] and [4] we applied these ideas to beamforming and showed how to carry out optimum beamforming in a coherent signal environment *without suffering signal cancellation*. Simulation studies were carried out for various scenarios including narrowband and broadband sources, different signal to noise ratios and several source and sensor directions to assess the performance of the new beamformer. The results have borne out theoretical predictions. Signal cancellation has been eliminated and effective nulling of coherent jammers obtained.

Some attractive features of spatial smoothing concept include simplicity, *low computational overhead* and robustness to actual degree of coherence.

2.1.2.3 Other Applications of Eigenstructure Methods

The eigenstructure methods have been applied to new problems in statistical signal processing. In [1] we discussed new methods to *resolve highly overlapping echoes*. The signal model is typical in radar and geophysics where repetitive observations are available of overlapped signals in additive noise. The performance of this new method has been most promising. Applications of this high temporal resolution technique to radar/sonar target imaging (for identification) and medical imaging are under investigation.

Another study [7] addresses source localization by widely spaced subarrays. Processing techniques which operate only on subarray covariances have been developed which outperform conventional triangularization methods. Moreover, consistent estimates for the number of sources are obtained.

In [2], some new concepts were reported for optimal beamforming in situations where one type of

interference (say directional jammers) are considered more undesired than say sensor to sensor uncorrelated noise. Eigenstructure methods have been used to build a modified beamformer with these desired properties.

2.1.3 Summary of Results

1. Derivation of a *consistent information theoretic* estimator for a number of sources.

2. A new method to *decorrelate* coherent wavefronts which can be applied to a wide range array processing methods to effectively solve this long outstanding problem.

3. New applications of eigenstructure concepts to resolving overlapping signals, source localization using subarray covariances and optimum processing when some interferences are more undesired than others.

2.1.4 References

1. Bruckstein,A. M. , Shan,T. J. and Kailath,T. The Resolution of Overlapping Echoes. submitted to *IEEE Trans. ASSP*

2. Citron,T. K. and Kailath,T. An Improved Eigenvector Beamformer. Proc. ICASSP, San Diego, CA, March, 1984, pp. 33.3.1-33.3.4.

3. Shan,T.J. , and Kailath,T. A New Adaptive Antenna System for Coherent Signals and Interference. 17th Asilomar Conference on Circuits, Systems and Computers, Monterey, CA, October, 1983.

4. Shan,T. J. and Kailath,T. Adaptive Beamforming for Coherent Signals and Interference. ASSP Spectrum Estimation Workshop II, Tampa, FL, November, 1983.

5. Shan, T.J., Wax,M. and Kailath,T. Spatial Smoothing Approach for Location Estimation of Coherent Sources. 17th Asilomar Conference on Circuits, Systems and Computers, Monterey, CA, October, 1983.

6. Wax, M. and Kailath,T. Determining the Number of Signals by Akaike's Information Criterion. Proc. ICASSP, San Diego, CA, March, 1984, pp. 6.3.1-6.3.4.

7. Wax,M. and Kailath,T. A New Approach to Decentralized Array Processing. Proc. ICASSP, San Diego, CA, March, 1984, pp. 40.7.1-40.7.4.

2.1.5 Recent JSEP Publications

Journal Papers

1. Egardt,B., Kailath,T. and Reddy,V. U.. "High-Resolution Spectral Analysis using Multi-Step Adaptive Prediction," *Circuits, Systems and Signal Processing* 2, 4 (1983), 422-443.

2. Kailath,T., Ljung,L. and Morf,M. "Recursive Input-Output and State-Space Solutions for Continuous-Time Linear Estimation Problems." *IEEE Trans. Autom. Contr. AC-28*, 9 (September 1983), 897-906.

3. Kwon,W. H., Bruckstein,A. M. and Kailath,T. "Stabilizing State-Feedback Design via the Moving Horizon Method." *Int. J. Control 37*, 3 (March 1983), 631-643.

4. Lev-Ari,H. and Kailath,T. "Lattice Filter Parametrization and Modeling of Nonstationary Processes." *IEEE Trans. Inform. Thy. IT-30*, 1 (January 1984), 2-16.

5. Samson,C. and Reddy,V. U. "Fixed Point Error Analysis of the Normalized Ladder Algorithm." *IEEE Trans. on ASSP ASSP-31*, 5 (October 1983), 1177-1191.

6. Wax,M. "Position-Location from Sensors with Position Uncertainty." *IEEE Trans. AES 19*, 5 (September 1983), 658-602.

7. Wax,M. and Kailath,T. "Optimum Localization of Multiple Sources in Passive Arrays." *IEEE Trans. ASSP* (October 1983).

8. Wax,M. and Kailath,T. "Efficient Inversion of Toeplitz-Block Toeplitz Matrix." *IEEE Trans. ASSP ASSP-31*, 5 (October 1983), 1218-1221.

Conference Papers

1. Citron,T. K. and Kailath,T. Eigenvector Methods and Beamforming A First Approach. 17th Asilomar Conference on Circuits, Systems and Computers, Monterey, CA, October, 1983.

2. Citron,T. K. and Kailath,T. An Improved Eigenvector Beamformer. Proc. ICASSP, San Diego, CA, March, 1984, pp. 33.3.1-33.3.4.

3. Kailath,T. Estimation and Control in the VLSI Era. The 22nd IEEE Conf. on Decision & Contr., San Antonio, TX, December, 1983.

4. Lev-Ari,H. and Kailath,T. Spectral Analysis of Nonstationary Processes. IEEE Inter'l. Symp. on Inform. Thy., St. Jovite, Quebec, Canada, Sept., 1983. Abstract

5. Reddy,V. U., Shan,T-J. and Kailath,T. Application of Modified Least-Square Algorithm to Adaptive Echo Cancellation, 1983 ICASSP, Boston, MA, April, 1983, pp. 53-56.

6. Shan,T. J. , and Kailath,T. A New Adaptive Antenna System for Coherent Signals and Interference. 17th Asilomar Conference on Circuits, Systems and Computers, Monterey, CA, October, 1983.

7. Shan,T. J. and Kailath,T. Adaptive Beamforming for Coherent Signals and Interference. ASSP Spectrum Estimation Workshop II, Tampa, FL, November, 1983.

8. Shan,T. J. and Kailath,T. New Adaptive Processor for Coherent Signals and Interference. Proc. ICASSP, San Diego, CA, March, 1984, pp. 33.5.1-33.5.4.

9. Shan,T. J., Wax,M. and Kailath,T. Spatial Smoothing Approach for Location Estimation of Coherent Sources. 17th Asilomar Conference on Circuits, Systems and Computers, Monterey, CA, October, 1983.

10. Wax,M. and Kailath,T. Efficient Inversion of Doubly Block Toeplitz Matrix. 1983 ICASSP, Boston, MA, April, 1983, pp. 170-173.

11. Wax,M. and Kailath,T. Determining the Number of Signals by Information Theoretic Criteria. ASSP Spectrum Estimation Workshop II, Tampa, FL, November, 1983.

12. Wax,M. and Kailath,T. A New Approach to Decentralized Array Processing. Proc. ICASSP, San Diego, CA, March, 1984, pp. 40.7.1-40.7.4.

13. Wax,M. and Kailath,T. Determining the Number of Signals by Akaike's Information Criterion. Proc. ICASSP, San Diego, CA, March, 1984, pp. 6.3.1-6.3.4.

14. Wax,M. and Kailath,T. A New Approach to Decentralized Array Processing. Proc. ICASSP, San Diego, CA, March, 1984, pp. 40.7.1-40.7.4.

15. Wax,M., Kailath,T. and Schmidt,R. O. Retrieving the Poles from the Natural Response by Eigenstructure Method. The 22nd IEEE Conf. on Decision and Control, San Antonio, TX, December, 1983.

16. Wax,M., Shan,T-J. and Kailath,T. Covariance Eigenstructure Approach to 2-D Harmonic Retrieval. 1983 ICASSP, Boston, MA, April, 1983, pp. 891-894.

17. Wax,M., Shan,T-J. and Kailath,T. Covariance Eigenstructure Approach to Detection and Estimation by Passive Arrays; Pt. I: Direction-of-Arrival and Frequency Estimation of Multiple Narrowband Sources. IEEE International Symp. on Inform Thy., Canada, September, 1983.

18. Wax,M., Shan,T-J. and Kailath,T. Covariance Eigenstructure Approach to Detection and Estimation by Passive Arrays; Pt. II: Source Location and Spectral Density Estimation of Wideband Sources. IEEE International Symp. on Inform. Thy., Canada, September, 1983.

Accepted Papers

1. Bruckstein,A. M., Levy,B. C. and Kailath,T. Differential Methods in Inverse Scattering. Accepted for publication in *SIAM J. Appl. Math*

2. Kailath,T. and Wax,M. A Note on the Complementary Model of Weinert and Desai. accepted for publication in *IEEE Trans. Autom. Contr.*, Vol. AC-29, no.6

3. Lev-Ari,H., Cioffi,J. and Kailath,T. Least-Squares Adaptive-Lattice and Transversal Filters: A Unified Geometric Theory. Accepted for publication in special issue of *IEEE Trans. on Inform. Thy.*

4. Samson,C. Stability Analysis of Adaptively Controlled Not-Necessarily Minimum Phase Systems with Disturbances. accepted for publication in *Automatica*

5. Wax,M., Shan,T-J. and Kailath,T. Spatio-Temporal Spectral Analysis by Eigenstructure Methods. Accepted for publication in *IEEE Trans. ASSP.*

Submitted Papers

1. Bruckstein,A. M., Shan,T.J. and Kailath,T. The Resolution of Overlapping Echoes. submitted to *IEEE Trans. ASSP*

2. Shan,T. J. and Kailath,T. Adaptive Beamforming for Coherent Signals and Interference. submitted to *IEEE ASSP*

3. Shan,T. J., Wax,M. and Kailath,T. Eigenstructure Methods for Direction-of-Arrival Estimation of Coherent Sources. submitted to *IEEE Trans. ASSP*

4. Wax,M. and Kailath,T. Decentralized Processing in Passive Arrays. submitted to *IEEE Trans. ASSP*

Dissertations

1. Lev-Ari,H. *Nonstationary Lattice-Filter Modeling*. Ph.D. Th., Information Systems Laboratory, Department of Electrical Engineering, Stanford University, Stanford, CA, December 1983.

2.2 Signal Processing and Compression

Principal Investigators: R.M. Gray, M. E. Hellman, T.M. Cover, J. Gill

2.2.1 Scientific Objectives

The objective of this project is to study the basic limitations on the performance and efficiency of communication networks, including both multiuser and point-to-point systems. A parallel objective is to develop improved methods of signal processing for these systems from the structures used to verify the performance limitations. Attention will be directed toward the trade-offs between performance and complexity in signal-processing algorithms. Signal processing for data compression, improved signal-to-noise ratios, and classification will be investigated.

2.2.2 Progress

2.2.2.1 Vector Quantization

investigators: (R.M. Gray, P.C. Chang, T. Flynn)

During the past year the project has focused on three principal problems: The design of feedback vector quantizers for data compression, the design of adaptive vector quantizers for speech compression, and the extension of vector quantizer design algorithms to the design of combined quantization/classification distributed sensor networks.

- **Feedback Vector Quantizers:**

  A stochastic gradient algorithm for designing predictive vector quantizers (PVQ) was developed in order to get better codebooks and faster design speed. To further improve the performance, adaptive VQ's which combine the waveform coding techniques and linear predictive coding (LPC) techniques were studied.

  Predictive Vector Quantizers are vector generalizations of scalar predictive quantization or DPCM: a vector quantizer in a feedback loop quantizes the error between the new input vector and a reproduction vector predicted from past quantizer outputs. Both the predictor and quantizer operate on vectors. Because of the feedback loop, it is more complicated to design a locally optimum codebook for a PVQ than for a memoryless VQ. Cuperman and Gersho [3, 2, 5] designed a PVQ with two main steps: first a set of linear vector predictive coefficients was designed by generalized LPC techniques; then a codebook for these predictor coefficients was designed by the generalized Lloyd algorithm. The codebook obtained by this method may be locally optimum under the assumption of very small quantizer error. Unfortunately, this assumption is not valid for low rate coding. Furthermore, no procedures were given to improve the predictor for the quantizer, therefore, once the predictor coefficients are not optimum, the final codebook is nonoptimum.

Codebook and predictor design based on a stochastic gradient algorithm (or, equivalently, a generalized steepest descent algorithm) avoids these disadvantages: It simultaneously improves the linear predictive coefficients and the vector quantizer in the feedback loop iteratively for a given training sequence. This provides better performance and faster convergence. Preliminary results may be found in Gray [6].

- **Adaptive Vector Quantization for Speech:**

An adaptive vector quantizer is a system using a model classifier to adapt a waveform VQ so that the waveform codebook can be better matched to local behavior of speech, thereby achieving better reproduction quality. Both the adaptation information and waveform encoding result are sent to the receiver. The model VQ typically operates on a much larger vector of samples, e.g., 128 samples, and the codebook size of the model VQ is small, hence the number of bits spent on specifying the model through the side channel are typically much less than those devoted to the waveform coder.

We developed a simulated code design algorithms for several adaptive VQ's using a voice coding LPC VQ with an Itakura-Saito distortion and ordinary memoryless VQ's with squared error distortion for the data classified by the LPC VQ. Preliminary results and comparisons with other compression systems may be found in Gray [6].

- **Quantization and Classification in Distributed Sensor Networks:**

This work treats the problem of data quantization in distributed sensor (e.g., radar or sonar) systems. The sensors, at several widely separated locations, gather data which must be converted to digital form for communication to processing locations at which the digitized data are combined and the inference (e.g., detection, location, or classification) is done. The digitized data must be as informative as possible, subject to the limitations on data rate. The appropriate strategy is not to reproduce the original data waveform, but to preserve its sensitivity to the targets under observation.

The problems of detection and classification (in which one chooses among a finite number of alternatives) were formulated in a Bayesian fashion. Two methods of quantizer design were considered: one which makes small the exact expected cost, the other which makes small an upper bound expressed as a weighted sum of distributional overlap measures. The second method was motivated by the guidelines it provides for cooperation among sensor locations. In both methods, a quantizer is specified by a "codebook" of representative points and a distortion measure which dictates how data points are mapped into codewords; this form allows a prototype quantizer to be improved using an iterative algorithm similar to the Lloyd algorithm.

In problems of estimation (of a real vector parameter), attention was restricted to cases where the log-likelihood function induced by an observation can be treated as quadratic. (This is true, for example, for a strong known signal contaminated with Gaussian noise.) described in terms of them. The increase in mean-square estimation error due to quantization was found to be expressible (approximately) as a weighted mean-square error in the quadratic parameters. Using this, the established methods of quantization for minimum mean-square error can be applied to this problem.

2.2.2.2 Advances in Cryptography

Investigator: M.E. Hellman

In [4] we presented a public key distribution system which depended on the difficulty of computing discrete logarithms. Merkle [7] and [1] have found a faster, subexponential method for computing this function. In earlier work, we extended this algorithm from GF(q) to the more general case, GF(q**m) with q fixed and m tending to infinity. In doing this, we also found a way to rigorize the use of a precomputation, by defining a "virtual spanning set".

In recent work, we have extended the subexponential behavior to GF(q**2). This was an important step because it indicates that the discrete logarithm function is probably computable in subexponential time in general. At first we were only able to show the subexponential behavior for 99.8% of the primes q because not all quadratic fields possess the unique factorization property. But, by defining "super primes" to be quadratic primes which also have prime norm, we were able to circumvent this problem and extend the result to all primes q.

We also have developed a new digital signature scheme based on the discrete logarithm problem. The signature scheme differs from the RSA system in that it is not based on a public key cryptosystem.

2.2.2.3 Advances in Data Compression and Information Inequalities

Investigator: Thomas M. Cover

Our work covers several areas.

- **Multiple Descriptions:**

  In Cover and El Gamal, we present a rate region for the multiple descriptions problem. Here we wish to give two separate descriptions of a random variable such that each is good but together they are very good. Recently we have obtained partial results on the converse for such a rate region with Shen Shi Yi. We await further developments. Berger and Zhan Zheng have informally announced some results showing that the Cover/El Gamal region is only an inner bound rather than the true rate distortion rate region for this problem.

- **Hadamard:**

  We have found an unsuspected new proof of the classical Hadamard inequality that says that the determinant of a matrix is less than the products of the lengths of its rows. The three line proof follows from plugging the multivariate normal into the entropy inequality and represents the first new proof of this theorem in 30 years.

- **AEP**

  Our work on showing that there is an asymptotic equipartition property for multiplicative processes (like the stock market) is still in progress. The AEP first became known in statistical mechanics and was later used to good effect by Shannon in information theory. It states that with high probability, an ergodic source really consists of an almost uniform distribution over a small number of possible outcomes, hence the term "equipartition." Nicely enough, such an equipartition characterization is also true of an ergodic stock market. It is shown that the capital growth rate (rather than the entropy rate) tends to a limit characteristic of the market. This allows comparing compounding random processes by their growth rates rather than by looking deeply into the guts of the statistical time dependence.

- **Brunn Minkowski:**

  In the paper Costa/Cover, we show a direct analogy between the Brunn-Minkowski inequality for the volumes of set sums under addition and the deep entropy power inequality. The similarity is so striking that there must exist a common proof. Although we do not find such a proof, we exhibit new theoretical consequences of both inequalitities.

- **Burg's Theorem:**

  In Choi/Cover, currently scheduled to appear in IEEE Proceedings, we find a new four line proof that Burg's maximum entropy spectral density estimate is achieved by the appropriate Gauss-Markov process. This simplifies previous proofs which used irrelevant mathematics to establish the result. The proof is primarily information-theoretic and follows from the chain rule for entropies.

2.2.2.4 Data Compression for Computer Data Structures

investigators: J. Gill, K. Chu

In the past year, this project has evolved from primarily theoretical and software efforts concerned with compacting tree-like data structures. Our research has focused on the development of a hardware/software subsystem for compression of computer file systems. The goal of the subsystem, whose preliminary design was completed in February 1984, is to achieve a compression ratio of 50% at a data rate of 1 megabit/second. Although the specified data rate is an order of magnitude slower than that of typical computer disk subsystems, it is two orders of magnitude faster than that achievable by software-only approaches.

The data compression technique we have selected is a modification of the method of Ziv and Lempel [8, 9]. The implementation is an improvement of the suffix-tree approach of Rodeh, Even, and Pratt. The improved algorithm yields faster execution for the micro-coded compression engine that

we have designed, although the resulting compression ratio is somewhat poorer. The compression and expansion algorithms were first implemented in software using C programs running on the Vax 11/780 in the Information Systems Laboratory. In tests on more than 5 megabytes of text and binary data, we confirmed that a compression ratio of slightly more than 50% can be achieved.

An evaluation of the software versions of these compression algorithms revealed that the great majority of the execution time was spent in the relatively simple operation of following links in a suffix tree. Since these operations can be performed very rapidly by low cost special purpose hardware, we began a study of the feasibility of a hardware implementation of our improved suffix-tree construction. The basic hardware design, based on the AMD 29116 16-bit bipolar microcontroller and the AMD 2910 microprogram sequencer, was completed in February, as was the micro-instruction format for the compression engine. The prototype design comprises approximately 70 integrated circuits; most of the ICs are memory and latches, which allow the microprogram to be stored in RAM during subsystem development. The prototype compression unit is standalone; a revised version will be attached to the data bus of a small computer (IBM PC compatible), so that data transfers to/from the disk drive can be routed through the compression unit.

In summary, algorithms for compression of data in computer file systems have been developed and implemented in software. The preliminary design of a low-cost hardware implementation has been completed.

3. Summary of Results

Two new code structures and design techniques for these strucures were developed for data compression systems: predictive vector quantizers designed by stochastic gradient algorithms and adaptive vector quantizers using memoryless vector quantizers for both the classifier used to adapt and for the waveform coder. A new approach was developed to quantizing data in distributed sensor networks so as to best communicate the information relevant to other nodes' required decisions.

2.2.3 References

1. Adleman,L. A Subexponential Algorithm for the Discrete Logarithm Problem with Applications to Cryptography. Proc. IEEE 20th Annual Symp. on Found. of Comp. Sci., October, 1979.

2. Cuperman, A.V. and Gersho, A. Adaptive differential vector coding of speech. Conference Record, GlobeCom 82, December, 1982, pp. 1092-1096.

3. Cuperman, V. and Gersho, A. Vector predictive coding of speech at 16 Kb/s. Submitted for possible publication, 1983

4. Diffie,W. and Hellman,M. "New Directions in Cryptography." *IEEE Trans. on Information Theory* (November 1976).

5. Gersho, A. and Cuperman, V. "Vector Quantization: A pattern-matching technique for speech coding," *IEEE Communications Magazine* (December 1983).

6. Gray, R.M. "Vector Quantization." *IEEE ASSP Magazine* (April 1984).

7. Pohlig,S. *Algebraic and Combinatorial Aspects of Cryptography*. Ph.D. Th., Stanford University, Dept. of Electrical Engineering, 1977.

8. Ziv, J., and Lempel, A. "A Universal Algorithm for Sequential Data Compression." *IEEE Transactions on Information Theory IT-23* (May 1977), 337-343.

9. Ziv, J., and Lempel, A. "Compression of Individual Sequences via Variable-Rate Coding." *IEEE Transactions on Information Theory IT-24* (September 1978), 530-536.

2.2.4 Recent JSEP Publications

1. Costa, M. and Cover, T. On the Similarity of the Entropy Power Inequality and the Brunn Minkowski Inequality. Stat. Report #48, submitted as a Correspondence to IEEE Trans. on Information Theory, September 1983

2. Hayes,J.F., Cover,T. and Riera,J. "Optimal Sequence Detection and Optimal Symbol-by-Symbol Detection: Similar Algorithms." *IEEE Trans. on Information Theory COM-30*, 1 (January 1982), 152-157. supported by JSEP

3. Cover, T. "An Algorithm for Maximizing Expected Log Investment Return." *IEEE Trans. on Information Theory* (March 1984).

4. Cover, T. and El Gamal, A. "An Information Theoretic Proof of Hadamard's Inequality." *IEEE Trans. on Information Theory IT-29*, 6 (November 1983), 930-931.

5. Gray, R.M. "Vector Quantization." *IEEE ASSP Magazine* (April 1984).

6. Sabin, M.J. and Gray, R.M. Product code vector quantizers for waveform and voice coding. to appear in IEEE Transactions ASSP

7. Tao,B., Abut,H., and Gray,R.M. Hardware Realization of Waveform Vector Quantizers. to appear in IEEE Transactions on Communications. Partially supported by JSEP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